

Monthly Spotlight

[New \\$79 BeMicro SDK: Plug In to Your PC and Start Developing Code](#)

The new ultra-small BeMicro SDK is an easy-to-use evaluation platform that lets you create, compile, run, and debug a software project in a Nios® II processor in minutes. Attend a hands-on BeMicro workshop for only \$59 and get the kit free. [Learn more](#) and watch the [kit video](#).



FPGAs, CPLDs and ASICs

[Video: Achieving 25-Gbps Transceiver Performance on 28-nm FPGAs](#)

See 28-nm transceiver technology running a pseudo-random bit pattern at 25 Gbps. View eye diagrams across 10GBASE-KR backplane at 10 Gbps.



Software, Intellectual Property, and Development Kits

[New Embedded Initiative Delivers Single FPGA Design Flow](#)

With Quartus® II software, a new system-level integration tool, a common FPGA IP library, and a diversity of processors, you'll be able to efficiently develop and deploy configurable embedded systems. [Learn more](#).

[Download Quartus II v10.0 Service Pack 1](#)

SP1 includes many software and GUI enhancements, plus final timing and power models for many Cyclone® IV and all Cyclone III LS devices.



Technology and End Markets

[White Paper: Design with 28nm Variable-precision DSP Architecture](#)

Read about the DSP architecture of the latest 28-nm Altera® FPGAs and see how it enables efficient implementation of FIR filters and FFTs.

[White Paper & Webcast: Achieving 1 TeraFLOPS with 28-nm FPGAs](#)

Explore how floating-point technology can provide processing rates of 1 teraFLOPS on a single FPGA die. Read the [white paper](#) and watch the [webcast](#) to learn about our new fused datapath design flow.



Training & Events

[New Class: Advanced Timing Analysis with TimeQuest](#)

Learn to write SDC files to constrain advanced types of interfaces and blocks. Analyze these designs to verify operation and performance.

[Updated Class: Implement High-Speed Memory Interfaces w/FPGAs](#)

This instructor-led class focuses on interfacing to DDR3 memory using UniPHY. Get hands on experience with Stratix® III development kits.

[Updated Class: Quartus II Software Debug and Analysis Tools](#)

New labs cover SignalProbe, In-System Memory Content Editor and Chip Planner. Learn system debug with Virtual JTAG Interface and System Console.



[Click to enlarge](#)

[Visit Altera at MILCOM 2010, Oct 31 - Nov 3, San Jose, CA](#)

Visit our booth to see how Altera technology provides customizable, secure network connectivity for users and assets from the core to the edge.

[Register for Free Functional Safety Seminar at SPS Show, Germany](#)

Need IEC61508-compliant development flows, tool chains & devices? Take this TÜV Rheinland/Altera seminar Nov 23-24. Register now.

Altera In the News

[Next Generation Direct RF EdgeQAM Design](#), **FPGA Journal**

Read how to design and implement an all digital EQAM modulator using an FPGA for a direct RF DAC interface without expensive, bulky analog components.

[Simultaneous Multimode RRH Design Made Easy](#), **Wireless Design & Development**

Simultaneous multimode support is an emerging basestation requirement as operators transition networks between 2G, 3G, and 4G technologies.

Most Popular News from Last Issue

[7 Ways to Reduce Your Compilation Time](#)

Cut your compile times by using 7 techniques in this updated Quartus II Handbook chapter for version 10.0.

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