

Monthly Spotlight

[White Paper: BDTI's Analysis of Our Floating-Point DSP Design Flow](#)

Read BDTI's independent analysis of Altera's high-performance floating-point DSP design flow. This paper includes performance results, tool flow usability, and a matrix inversion floating-point design example. Also view the related [webcasts](#) and [online training](#).

Read BDTI's Analysis of Altera's Floating-Point DSP Design Flow



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FPGAs, CPLDs, and ASICs

[Webcast: Implementing Floating-Point DSP in an FPGA](#)

Learn to implement floating-point DSP on our FPGAs. See how our design flow overcomes implementation challenges.

[MathWorks/Altera Webcast: FPGA Design Using MATLAB & Simulink](#)

Oct 5, 6 a.m. and 11 a.m. PDT. In this introductory webcast see how you can reduce 33% – 50% of FPGA design time by adopting workflows based on MATLAB and Simulink.

FPGA Design Using MATLAB and Simulink



[Register For Webcast](#)

[Get the Latest BittWare COTS Board with a Stratix® V FPGA](#)

This board provides a flexible solution for high-performance signal processing and data acquisition. Visit [BittWare's website](#) for details.

[Design Embedded Systems with \\$79 DE0-Nano Development Board](#)

This compact board features the Cyclone® IV FPGA, and is perfect for sensing applications and portable designs that require low power. It is sold by Terasic for only \$79.

Take an Online Training Class for Free



Technology and End Markets

[White Paper: Designing Safe Industrial Systems on a Chip](#)

Learn how to save up to 18 months of design time using Altera's SIL3 Functional Safety Data Package to achieve TÜV product certification.

Training and Events

[Online Training: Command Line Scripting](#)

Learn about Quartus® II software command line scripting capabilities, including writing batch files, shell scripts, and makefiles to automate design flows.

[Online Training: Design High-Performance Floating Point with FPGAs](#)

In this free 1-hour training, learn how to structure, implement, and optimize floating-point applications for FPGA implementation.

[Schedule a Meeting with Us at MILCOM, Nov 7–10, Baltimore](#)

Visit booth 1703 to learn how FPGAs enable cyber security and information assurance from core to edge. Contact us at milcom@altera.com to reserve your meeting time.

[Meet Us at SPS/IPC/DRIVES, Nov 22–24, Germany, Hall 6, Stand 111](#)

Learn how Altera® FPGAs enable efficient and safe drive systems. Register for free functional safety and motor control design methodology

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workshops.

Altera in the News

[Faster Floating-Point](#), **EE Journal**

Read Kevin Morris' commentary on the long history of attempts to use FPGAs for floating-point designs and see why it is now a reality.

Most Popular News from Last Issue

[Using the Nios II Processor—Free Online Training](#)

Are you new to the Nios® II processor? Invest 90 minutes in technical training to learn key best practices for the processor and its tools.

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