

December 2006: Altera's net seminar monthly e-newsletter provides schedules and descriptions of upcoming and recently broadcast Altera® online seminars.

You've heard about Stratix III FPGAs. Now find out what the buzz is about.



[Overview of Altera's 65-nm Stratix III FPGAs](#) **Free**

Duration: 15 minutes
View On-Demand Now!

In this QuickCast, Jordon Plofsky, Altera's Senior Vice President of Marketing, and Brad Howe, Altera's Vice President of IC Design Engineering, discuss how Altera's Stratix® III 65-nm high-end FPGAs meet product and engineering management's business and technical requirements.

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[Using Stratix III FPGAs to Achieve Higher Performance Systems with Lower Power](#) **Free**

Duration: 60 minutes
View On-Demand Now!

Design your next-generation high-end system with confidence. Learn how Stratix III FPGAs, with Programmable Power Technology, deliver maximum power when needed to performance critical paths in the design, and low power everywhere else. Discover how the use of performance-optimizing Quartus® II development tools and EDA synthesis support provide complete solutions for high-end system design.

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"Altera's [How to Break ASSP Time & Risk Design Barriers Net Seminar](#) was extremely helpful to me. It brought the experts from Altera directly to my desktop, giving training on specific topics and answering questions."

- Michael Li,
 Software Design Engineer, Thomson





[Accelerate IPTV Headend Design Using Available IP and Reference Designs Net Seminar](#) **Free**

Duration: 60 minutes
View On-Demand Now!

Designing an IPTV headend? This net seminar describes how using FPGAs with IP and reference designs can accelerate your designs and shorten time to market. You'll learn how to integrate available video encoder and data communication building blocks in your existing systems, accelerate system performance with optimized IP and reference designs, and more.

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[Code:DSP - Video, Image & Signal Processing Net Seminar Series](#) **Free**

Duration: 3 separate 60-minute sessions
View On-Demand Now!

Boost DSP performance and lower overall cost with the Code:DSP Video, Image and Signal Processing Net Seminar Series. Learn to design video, image and wireless-processing solutions using MATLAB/Simulink and DSP Builder/SOPC Builder. And, learn how to lower costs using Cyclone® II FPGAs and HardCopy® II structured ASICs. Hear from industry experts. Discover leading-edge solutions.

Code:DSP Net Seminar Series Highlights

Video Processing Tutorial with FPGAs
(Presented by The MathWorks & Altera)

IF Modem Design
(Presented by The MathWorks & Altera)

Multi-Channel H.264 Encoding Solution for Surveillance Applications
(Presented by 4i2i & Altera)

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Congratulations



Representing Altera, Kevin Johnson of Earle Associates, presents Jim Means, L3 Communications engineer, an Epson P-2000 Multimedia Viewer (\$500 US). Jim won it by attending [Part 3 of the Altera Stratix® II GX Seminar Series](#).

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