

Welcome to the January issue of Altera's monthly Net Seminar e-Newsletter. Each issue gives you information on upcoming & recently broadcasted net seminars.

January 2006

Free Upcoming Net Seminars & Net Seminar Series

Embedded SYSTEMS

Register Now

[Embedded Systems Development Net Seminar Series](#)

3 sessions in 2 different time zones. Register Now!

Free

Find out in this three-part Embedded Development Net Seminar Series how Altera's tools, FPGA devices, and the Nios® II processor are being used to develop lower-cost embedded solutions with higher performance, more features, and shorter development times.

[Register now for the sessions hosting live in your time zone!](#)

Upcoming Net Seminar Series Highlights

Part 1: Solving Embedded System Issues With FPGAs and Soft Processors

Date: Wednesday, January 25, 2006
 North America (Live): 11:00 AM Pacific Time
 Europe (Live): 1:00 PM Greenwich Mean Time
Win an RCA Lyra 20GB Audio/Video Jukebox (US\$400 value) built with Altera devices.

Part 2: Creating Enhanced Embedded Systems With FPGA Hardware Development Tools

Date: Wednesday, February 1, 2006
 North America (Live): 11:00 AM Pacific Time
 Europe (Live): 1:00 PM Greenwich Mean Time
Win a Pinnacle MovieBox Deluxe (US\$250 value) built with Altera devices.

I found the [Code: DSP Net Seminar Series](#) very informative. It gave me new ideas for reducing system cost & easing implementation. It was definitely worth the time & proved to be very useful for projects on the horizon.

Craig Windish, Hardware Engineer, Siemens



Part 3: Accelerating Software Development for Soft Processor and FPGA-Based Embedded Systems

Date: Wednesday, February 8, 2006

North America (Live): 11:00 AM Pacific Time

Europe (Live): 1:00 PM Greenwich Mean Time

Win a Pinnacle MovieBox Deluxe (US\$250 value) built with Altera devices.

[Win a Epson P2000 Multimedia Viewer \(US\\$500 value\), Built With Altera® Devices](#)

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Recently Broadcasted Net Seminars & Net Seminar Series



[Design ASSPs Faster With Structured ASICs](#)

Available Now! **Free**

Learn why it makes sense to develop your ASSP design with an FPGA, and how you can still have the option to use cost-reduced structured ASICs for volume production.



[Reduce FPGA Power With Automatic Optimization & Power-Efficient Design](#)

Available Now! **Free**

Find out about the automatic power optimization features of the PowerPlay technology in Quartus® II software. Learn about design techniques to further minimize power in FPGAs and methods to accurately estimate the power consumption of a design.



[Optimizing Signal Integrity in FPGA Applications](#)

Available Now! **Free**

Find out how to select the right FPGA that meets specific signal integrity requirements to ensure individual design success. Learn how to perform a thorough signal integrity assessment and understand the various factors that



need to be taken into consideration.

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Congratulations



Eric Mastromarchi (left), a hardware engineer for Lucent Technologies, recently won a Gateway DVD Recorder, built with Altera devices, by viewing the [FPGA Power Solutions for Leading-Edge FPGAs](#) net seminar live. Congratulations, Eric!

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