

December 2007: Altera's monthly Webcast newsletter provides schedules and descriptions of upcoming and recently broadcast Altera® online seminars.



Implementing High-Speed DDR3 Interfaces Free

Duration: 30 minutes
View Now, On Demand!

With today's requirements for high-speed memory interfaces surpassing 1 Gbps, FPGA silicon and IP must be designed to provide robust signal integrity and address the challenges of implementing DDR3 interfaces. Simulation still plays an important role in validating signal levels and timing margins.

In this webcast, you'll learn:

- The JEDEC requirements for DDR3
- How to address read/write leveling in your system
- How to reduce power consumption on your board and track PVT

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Signal and Power Integrity Design Techniques
for SSN Free

Duration: 40 minutes
View Now, On Demand!

This webcast teaches signal integrity design techniques to mitigate SSN, including how to maintain power integrity. You'll learn about measurement criteria, measured results, and data on design prototypes and simulation predictions.

In this webcast, you'll learn how to:

- Identify SSN mechanisms
- Quantify SSN as a percentage of signal swing
- Improve SSN on your system

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Webcast
 Reconfigure Transceivers Dynamically
 ▶ [View the Webcast](#)



Webcast
 Designing Multiservice Access Nodes for Cost, Power, and Features
 ▶ [View Now](#)



Webcast
 Plug & Play Signal Integrity
 ▶ [View the Webcast](#)



[Plug & Play Signal Integrity](#) **Free**

Duration: 15 minutes

View Now, On Demand!

A challenge facing designers of new backplane systems is to ensure reliable data transmission through complex backplane channels. In systems with multiple transceivers and backplane slots, designers face the daunting task of optimizing the signal integrity settings for every channel and every card slot in the backplane system.

In this webcast, you'll learn:

- About high-speed protocol trends
- About the challenges of designing high-speed backplanes
- How Altera's Plug & Play Signal Integrity can help you with your backplane designs using multi-gigabit transceivers

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[Cut Power 100X Using CPLD Coprocessors in Portable Applications](#) **Free**

Duration: 30 minutes

View Now, On Demand!

See how designers of low-power, portable electronic products can cut their design's power consumption by 100X with the new "zero-power" MAX IIZ CPLDs. This 30-minute webcast gives concrete examples on how to use CPLDs as coprocessors to manage and reduce power consumption in portable applications.

In this webcast, you'll learn:

- How a CPLD can be used as a low-power media coprocessor to reduce system power by as much as 100X
- Nine standard system functions where using a CPLD can reduce power in portable applications
- Three specialized applications that will benefit from using CPLDs

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[Dynamically Reconfigure Transceivers for Multiple Data Rates and Protocols in FPGAs](#) **Free**

Duration: 15 minutes

View Now, On Demand!

Designers are faced with the challenge of designing systems that support the newer and faster serial protocols while continuing to support slower legacy versions. Dynamic reconfiguration delivers an elegant solution to this challenge. With dynamic reconfiguration, Stratix® II GX FPGAs with embedded transceivers are the Swiss Army Knife of high-speed serial protocols.

In this webcast, you'll learn:

- About high-speed connectivity trends
- How to support multiple rates and protocols on FPGAs with embedded transceivers
- How dynamic reconfiguration can increase productivity for you and your customers

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[Designing Multiservice Access Nodes for Cost, Power, and Features](#) **Free**

Duration: 40 minutes

View Now, On Demand!

This webcast presents some FPGA-based solutions to the challenges of designing multiservice access nodes (MSAN).

After viewing this webcast, you will:

- Understand how to meet cost, power, and feature objectives for your MSAN application
- Be aware of the pre-built and building-block solutions that can accelerate your design process
- Learn about the cost advantages programmable logic can bring to an MSAN architecture

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