

**February 2007:** Altera's monthly net seminar e-newsletter provides schedules and descriptions of upcoming and recently broadcast Altera® online seminars.

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### [Customizing ASSPs for Consumer Electronics](#) **Free**

Duration: 60 minutes

**View Now, On Demand!**

Success in consumer electronics depends on the rapid introduction of innovative, feature-rich, competitively differentiated products. Off-the-shelf chipsets (ASSPs) are an excellent choice for achieving high feature integration. Programmable logic can then be used to provide a fast, low-risk, inexpensive path to the customization necessary for market success.

[Back to Top](#)

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### [Reducing FPGA Design Compile Times with Quartus II v6.1 Software](#) **Free**

Duration: 60 minutes

**View Now, On Demand!**

As designs become more complex and FPGA densities increase, it's important to know how your tools can reduce compile times for faster timing closure. Incremental compilation, a feature that enables advanced flows to achieve  $f_{MAX}$  gains, targets specific design areas while preserving performance in the areas of the design that haven't been changed.

This net seminar introduces incremental compilation and describes how to use it to shorten overall design time.

[Back to Top](#)

[“The Code:DSP - Video, Image, and Signal Processing Net Seminar Series](#) is extremely helpful in providing information to help system engineers get an overall perspective on how a product can be realized by using the Altera line of products... After seeing the seminars, I have a better understanding on which Altera product to use and what partner company to work with that will produce a system with the minimal amount of integration time.”

- Brandon Gushiken,  
Engineer, Trex Hawaii





## [Learn About High-Speed Clocking Architecture and Oscillator Selection for FPGAs](#) Free

Duration: 60 minutes  
**View Now, On Demand!**

There's little room for clock uncertainties and variations in high-speed or wide-bus interfaces, such as gigabit transceiver or high-speed memory interfaces. This net seminar covers various clock network topologies for FPGAs as well as a detailed discussion of jitter, its components, and its causes. In addition, guidelines on selecting the right oscillator for your high-speed design are provided.

[Back to Top](#)

### Congratulations



Representing Altera, Gord Leddy of Future California Electronics, presents Dennis Cote, Harding Instruments engineer, an Epson P-2000 Multimedia Viewer (US\$500). Dennis won it by attending the [Learn Best Board Design Practices for Power Delivery Network](#) net seminar.

[Back to Top](#)

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