

Partial Reconfiguration Design Flow

- Quartus II software will offer new tools with intuitive interfaces and simplified methodology to build the different design personas



[Webcast: Learn About Easier-to-Use Partial Reconfiguration Flow](#), 15 minutes

Watch this webcast to learn how Altera's new 28-nm Stratix® V FPGAs support partial reconfiguration. Find out how you can use the flow to develop more cost-effective designs for applications like optical transport network (OTN) multiplexing transponders and software-defined radio.

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[Webcast: Reducing Power and Cost of 6G Transceiver-Based Applications](#),

25 minutes

Need to strike the right balance between FPGA density, transceiver speed, cost, and power? Watch this webcast to learn which Arria II FPGAs are ideal for applications in the wireless, wireline, storage, and test industries. You'll also learn about two dev kits that give you resources to start designing with Arria II FPGAs today!

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[Webcast: Achieving 800-MHz DDR3 Performance With Advanced Silicon and Memory IP](#), 20 minutes

Watch this webcast to learn how our external memory solutions are faster, better, and easier to use. See how you can achieve higher productivity with our memory solutions, and also meet the demanding higher memory bandwidth and greater performance of FPGA applications.

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[Webcast: Achieve Lower Total Cost of Ownership for Industrial Designs](#),

25 minutes

Watch this webcast to learn how Altera industrial solutions deliver the capabilities you need to achieve your total cost of ownership (TCO) goals using a common FPGA platform. Also, learn how to use the same FPGA design to deploy multiple products for a faster time to market.

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[Webcast: Accelerate Your FPGA-based DSP Designs](#), 30 minutes

Watch this webcast to learn about Altera's total DSP portfolio at 28 nm. It'll speed up the design cycle for your FPGA-based applications. Also, watch how the DSP Builder tool creates fMAX and latency-optimized netlists automatically from MATLAB/Simulink design descriptions.

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