

**Quartus II Software's Incremental Compile**

Reduce Compile Times up to 75%—  
Compile Only File Changes

**[Webcast: Enhance Your Productivity with Faster Design Compile Times,](#)**

18 minutes

When choosing your FPGA design software, consider compile time, a key productivity advantage. In this webcast, you'll learn how Altera's Quartus® II design software delivers a 2X to 3X compile time advantage over competitive software.

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**[Video: 5 Reasons to Put Your Processor on an FPGA,](#)**

9 minutes  
Watch this video to understand five key reasons to put your processor on an FPGA. The video shows the ultra-small BeMicro SDK in action with the Eclipse IDE and Nios® II Embedded Design Suite. You'll see how easy embedded design on an FPGA can be with software tools you already know.

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**Image Processing IP: Fisheye Correction**

- A real-time image processing solution that:
  - Operates in a video camera's video input lane
  - Converts the video angle into "fish-eye" 180-degree view
  - Displays the resulting image on a TFT LCD
- **Multiple Values**
  - Allows independent camera with single lens or lens to be used
  - Camera selection and all processing from a single block of logic
- **Applications:**
  - Automotive backup cameras, video cameras
  - Monitoring video surveillance cameras

**[Webcast: Designing an IP Camera with a Single, Low-Cost FPGA,](#)** 20 minutes

Developing network surveillance cameras? Watch this webcast to see how an FPGA provides a single-chip platform for these cameras. Learn about a full video surveillance solution including silicon and intellectual property (IP) cores.

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**[Video: Easily Support WDR CMOS Image Sensor Processing with Low-Cost FPGAs,](#)** 7 minutes

Watch this video to learn how Cyclone® III FPGA performs system tasks to transform the sensor's RAW image data into the digital video interface (DVI) output format. See a demo of the Aptina MT9M033 720p WDR CMOS image sensor, image processing IP from Apical Ltd., and the Cyclone III FPGA Development Kit.

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**Bandwidth, Power, and Stratix Series FPGAs**

Delivering Higher Bandwidth at Lower Total Power

**[Webcast: Lower Power and Boost System Performance with 28-nm FPGAs,](#)** 40 minutes

Learn about key innovations in Stratix® V FPGAs that address bandwidth and power challenges in high-end systems designs. Find out how Embedded HardCopy® Blocks, power-efficient 28-Gbps transceivers, and software power optimization will help you meet your requirements.

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