

Results for oc_or1k OpenCore Design

In **Figure 1**, the Y-axis shows the f_{MAX} achieved on Altera® Stratix® III FPGAs and the nearest competing device. The x-axis shows the number of cores stamped for the oc_or1k OpenCore design. To increase the design size (and utilization), the number of stamps instantiated in the FPGA for each core was increased, resulting in a more rapid performance degradation on the nearest competing device.

Figure 1. f_{MAX} vs. design size (% utilization)

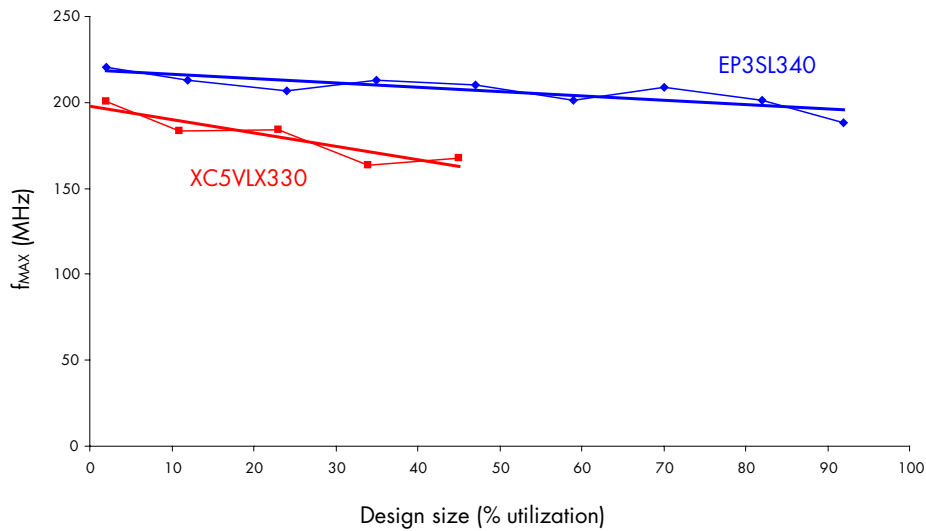


Figure 2 shows the maximum number of cores that can be instantiated in the FPGA core. Stratix III FPGAs can fit up to 40 cores (92% utilization), versus the 20 cores (45% utilization) fit by the nearest competing device.

Figure 2. Design size (% utilization) vs. number of cores

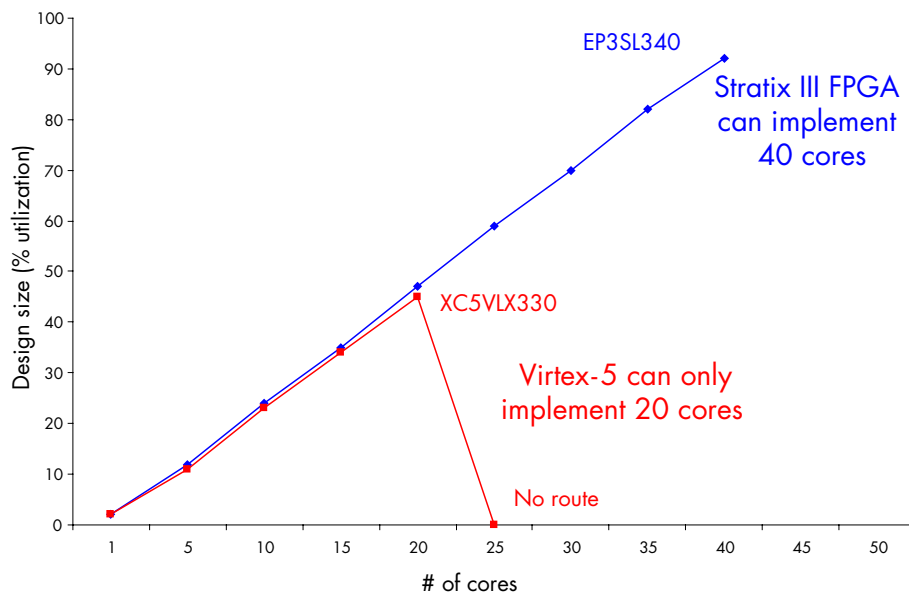
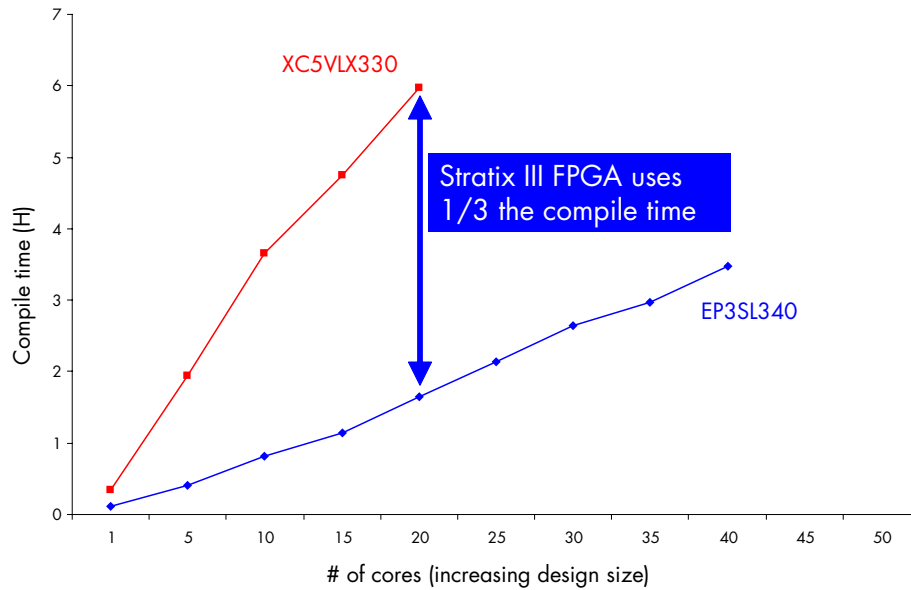


Figure 3 shows that Stratix III FPGAs compile in one-third the time as compared to the nearest competing FPGA. The compile-time comparison is based on the largest number of cores that can fit the nearest competing FPGA.

Figure 3. Compile time (H) vs. number of cores instantiated



For further information, visit the OpenCore website at www.opencore.org or Altera's "OpenCore Designs Validate—Stratix III FPGA Advantages Increase with Design Size" web page at www.altera.com/products/devices/stratix3/overview/architecture/performance/st3-opencores.html.



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