HST Jitter and BER Estimator Tool User Guide for Stratix IV GX and GT Devices

101 Innovation Drive
San Jose, CA 95134
www.altera.com

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1. HST Jitter and BER Estimator Tool for Stratix IV GX and GT Devices

This user guide describes Altera's high-speed communication link design toolkit (HST) jitter and bit error rate (BER) estimator tool, which was developed to comprehend jitter and horizontal eye opening to ensure that a high-speed link is interoperable at a target BER level. This tool provides BER estimation when the jitter components of the link subsystems are given, as well as optimize the channel design by either using the jitter margin in the transmit and receive devices for both cost and performance, or by quantifying the transmit and receive jitter margin in terms of BER enhancement. For Altera® Stratix IV GX and GT devices, this tool uses a characterized database.

Any communication link is composed of three key subsystems—the transmitter (TX), receiver (RX), and channel (CH) in between them. Communication link transmission reliability is measured in BER. BER is defined as the ratio of the total number of error bits received to the total number of bits transmitted across the link. In a high-speed serial link, jitter is the dominant contributor of the system BER from all the subsystems. Jitter can be separated into two distinct components—deterministic jitter and random jitter. Deterministic jitter is bounded and random jitter is unbounded.

The HST jitter and BER estimator tool treats the jitter caused by the transmitter, receiver, and channel statistically by convolving their corresponding probability density functions. The jitter probability density function is further simplified with the dual dirac model quantifying deterministic jitter with a peak-to-peak value and random jitter with a Gaussian root mean square. The deterministic and random jitter values for TX and RX are measured across various transceiver use conditions, including the output differential voltage level, process, voltage, and temperature (PVT) variations, channel-to-channel variations, worst-case core logic fabric noise, crosstalk coupling from the neighboring transceiver I/Os, single-ended I/Os, and LVDS I/Os.

A database of jitter characteristics for Altera Stratix® IV GX and GT devices is selectable from the HST jitter and BER estimator tool based on the measurement conditions. For a custom device, you must provide the deterministic jitter (DJ) and random jitter (RJ) input of the TX or RX. For selected input settings, if the jitter measurement data is not available, the tool interpolates and/or extrapolates the jitter characteristics based on the closest available data points in the jitter database. The HST jitter and BER estimator tool contains an integrated link simulator to estimate the non-equalizable channel deterministic jitter for a given channel's S-parameters based on Altera models, or you may manually enter the channel deterministic jitter value to estimate the link BER.

HST Jitter and BER Estimator Tool

The HST jitter and BER estimator tool predicts the link BER based on the characterized statistical data for protocol compliance. This spreadsheet tool explores the various "what-if" scenarios to estimate the allowable jitter margin of the subsystems. Also, you can use the HST jitter and BER estimator tool to optimize the channel design between the transmitter and the receiver.

The HST jitter and BER estimator tool contains the following files and folders:

- **Jitter_BER_Estimator_Tool**
  - **Jitter_BER_Estimator_Tool.xls**
  - **link_sim** (use the link simulator to estimate channel deterministic jitter. This option is available if both the TX and RX are Stratix IV GX or GT devices)
  - **channel1.s4p** (the sample tyco 30” legacy backplane channel S-parameters of type 2 network topology)
- **License Agreement.doc**
- **README.txt**
- **MATLAB_Component_INSTALL**
  - **MCRInstaller.exe**

The HST jitter and BER estimator tool is available through myAltera at the Altera Support Center.

For more information about the HST jitter and BER estimator tool, refer to *AN 608: HST Jitter and BER Estimator Tool for Stratix IV GX and GT Devices*.

Installing the MATLAB Runtime Installer

The `link_sim` tool requires that you install the MATLAB components provided with the kit. This installation does not require a MATLAB license to run.

To install the MATLAB components, follow these steps:

1. After unzipping the design kit, go to the MATLAB component INSTALL directory in the installation path and click **MCRInstaller.exe**

   C:\<install_directory>\<HST_Jitter_and_BER_Estimator_Tool_Kit> \MATLAB_Component_INSTALL**MCRInstaller.exe**

2. Follow the standard installation steps through the MATLAB Component Runtime Installer.

   This is a one-time installation. The installation process takes approximately five minutes to complete. After the installation finishes, you are ready to run the simulator in full-link and far-end mode to estimate the non-equalizable channel deterministic jitter.

Setting Up the HST Jitter and BER Estimator Tool

The HST jitter and BER estimator tool is a spreadsheet-based calculator with an internal characterization database. There are two parts to the HST jitter and BER estimator tool:

- Jitter and BER estimator—this spreadsheet is the main interface of the HST jitter and BER estimator tool. This user guide describes how to use the HST jitter and BER estimator tool.
- Characterization database—this database is composed of the statistical distribution of Stratix IV GX and GT jitter characterization data sets over PVT and various TX and RX operation conditions. The distribution covers the measured worst case jitter for the TX and RX and the data is embedded in the tool. The appropriate values are populated when you select a device and include the measurement conditions.

Figure 1–1 shows the HST jitter and BER estimator tool spreadsheet. There are three sections to the spreadsheet:

a. Global parameters (highlighted in red)—where you enter the target BER, data rate, and pattern.

b. Link configuration (highlighted in green)—where you select the analysis mode and configure the TX, RX, and channel subsystems.

c. Results (highlighted in pink)—where the total jitter (TJ) margin at the target BER and actual BER are calculated for your selected analysis mode. If you select full-link mode in the link configuration, the maximum allowable channel's deterministic jitter, TX jitter, and RX jitter are calculated.

☞ All the inputs to the HST jitter and BER estimator tool spreadsheet are colored in white. Measured data is displayed in blue. After the tool interpolates and/or extrapolates the jitter characteristics, the data is displayed in turquoise (light blue).

Figure 1–1. HST Jitter and BER Estimator Tool *(Note 1)*

Note to Figure 1–1:

(1) a = Global Parameters, b = Link Configuration, and c = Results.

HST Jitter and BER Estimator Tool Configuration

To configure the HST jitter and BER estimator tool, follow these steps (the details of each step are explained in subsequent sections):

1. Configure the global parameters. Set the **Target BER**, **Data Rate**, and **Test Pattern** options. Refer to "Step 1: Global Parameters".
2. Set the analysis mode to either **Full Link**, **Near-End**, or **Far-End**. If you select the **Near-End** or **Far-End** option, also enter the horizontal eye width opening mask. Select the TX measurement CDR bandwidth setting and non-equalizable channel deterministic jitter source to either manual or simulation. Refer to "Step 2: Link Configuration" on page 1–6.
3. Select the **TX Settings** option. Refer to "Step 3: TX Subsystem Setup" on page 1–9.
4. Select the **RX Settings** option. Refer to "Step 4: RX Subsystem Setup" on page 1–11.
5. Manually enter the channel deterministic jitter in the **Subsystem Jitter** option or run the link simulation to estimate the channel deterministic jitter in full-link or far-end mode. Refer to "Step 5: Channel Subsystem Setup" on page 1–12.
6. Analyze the results. Refer to "Step 6: Results" on page 1–16.

The results reflect any update(s) to the global or link configuration parameters.

Step 1: Global Parameters

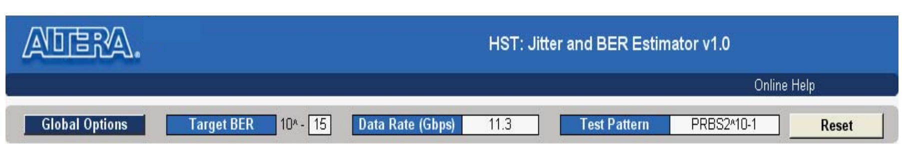
Figure 1–2 shows the global parameter options in the HST jitter and BER estimator tool. Global options include **Target BER**, **Data Rate (Gbps)**, and **Test Pattern**.

To perform the link analysis, you must enter the **Target BER**, **Data Rate** (in Gbps), and **Test Pattern** values. To enter the **Target BER**, enter an integer value between 2 and 19. These values depend on the link protocol requirements.

To make your selections for the **Data Rate** and **Pattern Selection** options, use the drop down menus. In addition to the data rate values listed in the drop down menu, you can also enter any value between 3.125 and 11.3 Gbps. The HST jitter and BER estimator tool interpolates and/or extrapolates based on the settings you entered.

For the Stratix IV GX device, use a data rate between 3.125 and 8.5 Gbps. For a Stratix IV GT device, use a data rate between 6.375 and 11.3 Gbps. For the **Test Pattern** option, select either **PRBS7** or **PRBS10** (Figure 1–2). The data rate restrictions are due to the characterized data set, not due to a device limitation.

Figure 1–2. Global Parameters

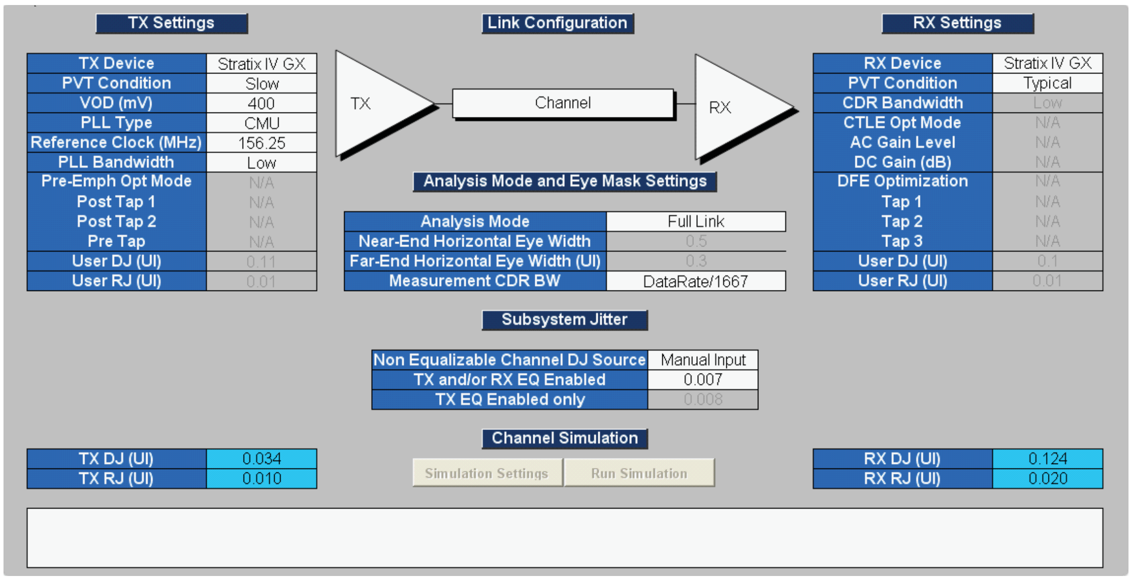


The HST jitter and BER estimator tool uses the interpolation method for both TX and RX when the measured data of the **Data Rate (Gbps)** option is not available in the database. In this case, the TX reference clock parameter is grayed out.

Step 2: Link Configuration

Figure 1–3 shows the link configuration section in the HST jitter and BER estimator tool.

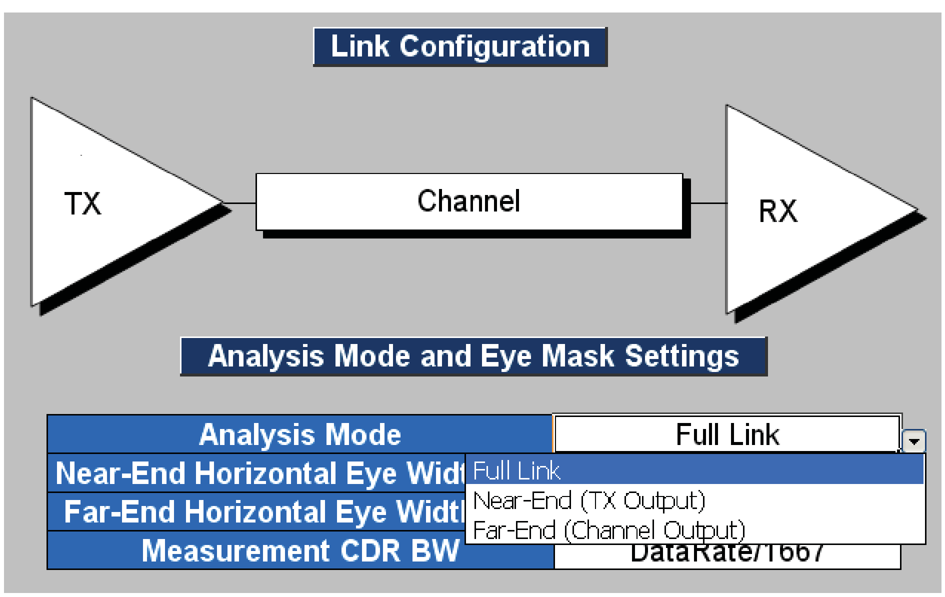
Figure 1–3. Link Configuration



Configure the link subsystems' settings based on your Analysis Mode selection. The **Analysis Mode** options are **Full Link**, **Near-End (TX output)**, and **Far-End (channel output)**.

Select the **Analysis Mode** option. Figure 1–4 shows the modes available for analysis.

Figure 1–4. Analysis Modes



Full-Link Mode

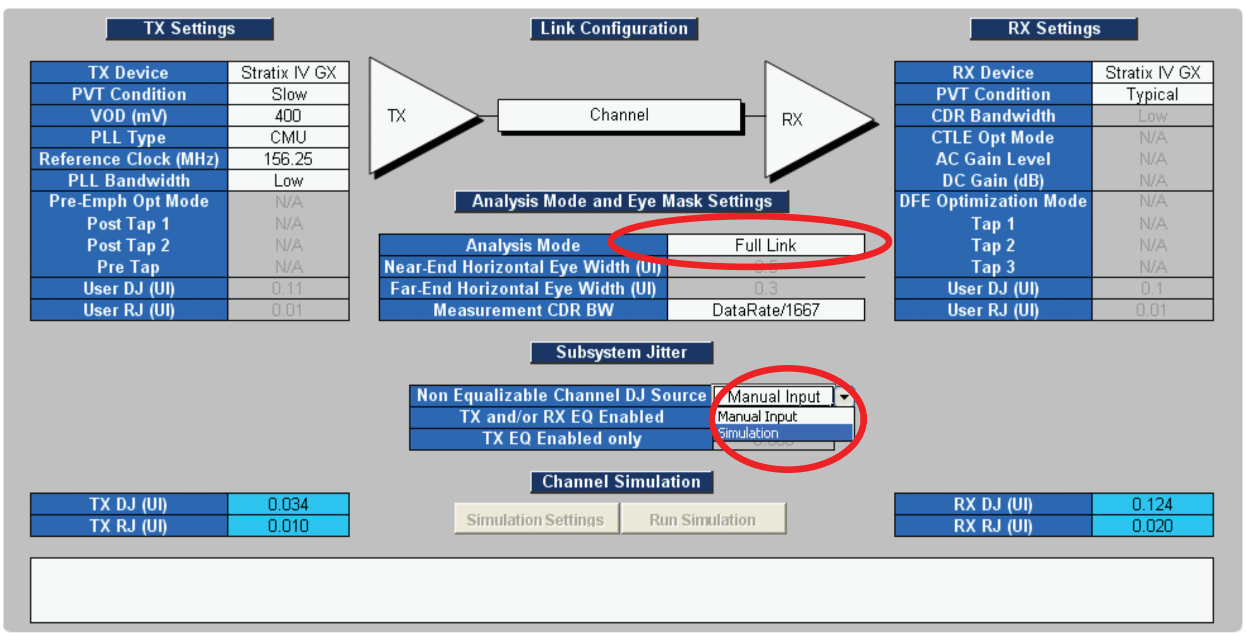
Full-link mode includes the TX, RX, and channel subsystems. In full-link mode, the tool analyzes the:

- Maximum allowable channel deterministic jitter and random jitter
- Allowable TX deterministic jitter and random jitter
- Allowable RX deterministic jitter and random jitter
- TJ margin at the target BER
- BER bathub curve and actual BER

In full-link mode, you must enter the non-equalizable channel deterministic jitter or use the integrated link simulator to estimate the non-equalizable channel deterministic jitter.

Figure 1–5 shows the **Non Equalizable Channel DJ Source** options, which are **Manual Input** and **Simulation**.

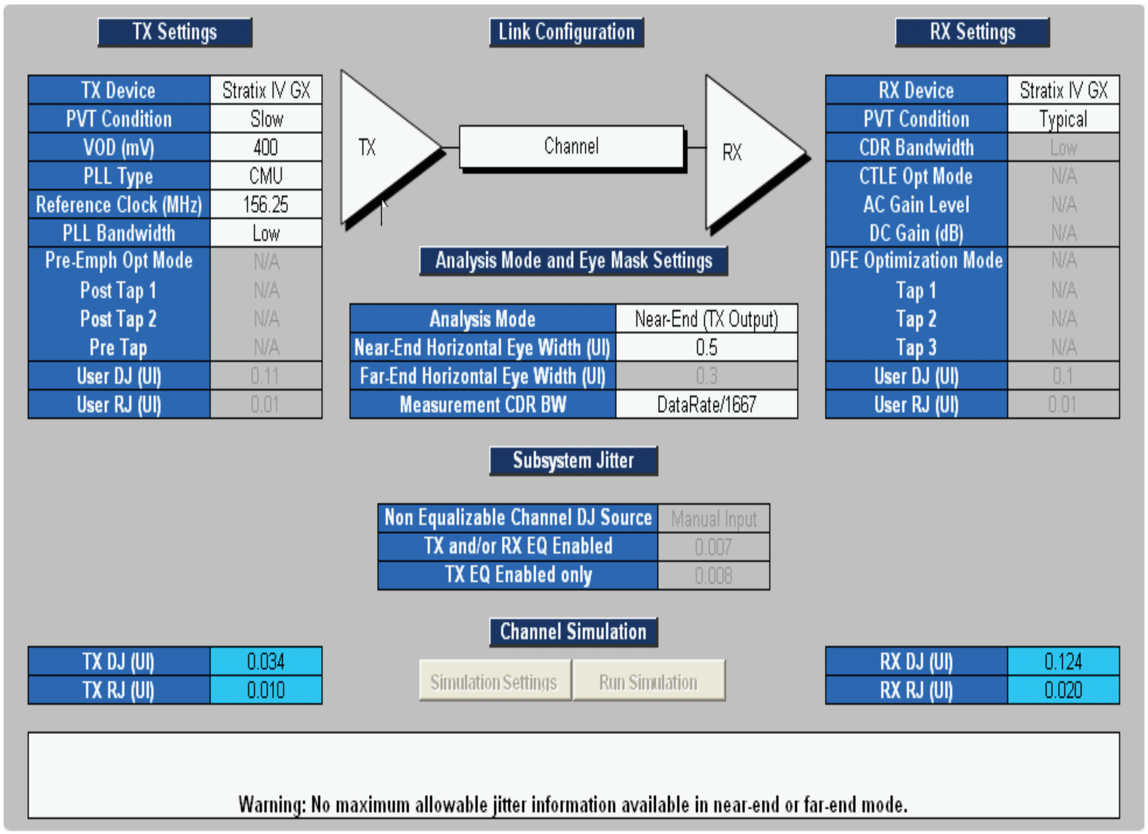
Figure 1–5. Full-Link Mode



Near-End Mode

Near-end mode includes the TX subsystem only. In near-end mode, you must enter the **Near-End Horizontal Eye Width (UI)** mask value, as shown in Figure 1–6. In this mode, the tool analyzes only the TX subsystem for the TJ margin for the specified mask value at the target BER and the actual BER at the TX output.

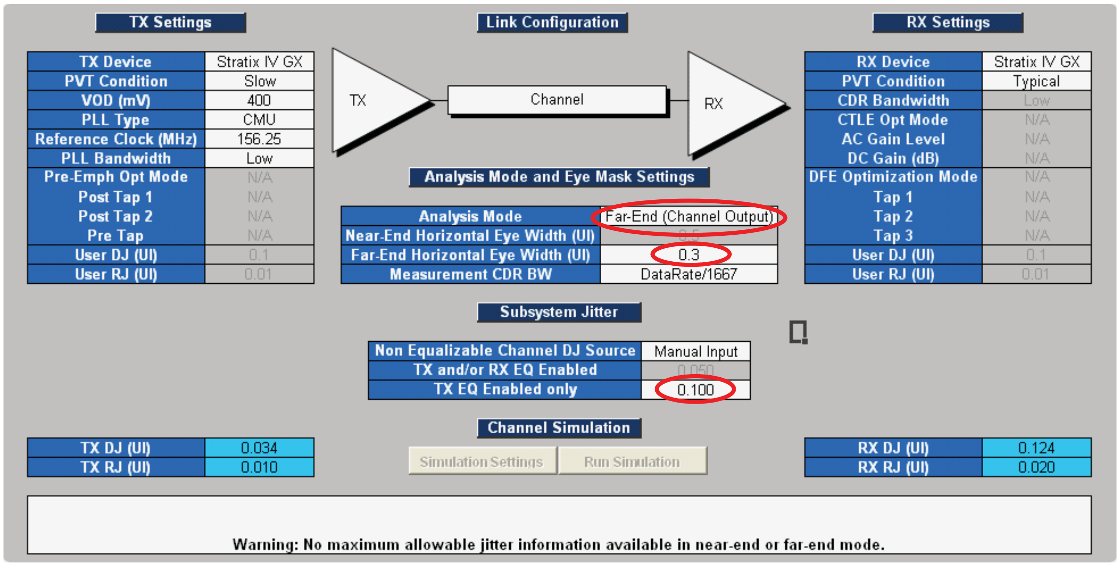
Figure 1–6. Near-End Horizontal Eye Width Mode



Far-End Mode

The far-end mode includes the TX and channel subsystems. In far-end mode, you must enter the **Far-End Horizontal Eye Width (UI)** mask value and the **Non-Equalizable Channel DJ Source** value. The **Manual** and **Simulation** options are available to account for non-equalizable channel deterministic jitter. Figure 1–7 shows the **Manual** option. In far-end mode, the tool analyzes only the TX and channel subsystems for the TJ margin for the specified mask value at the target BER and the actual BER at the channel output.

Figure 1–7. Far-End Mode



Measurement CDR Bandwidth

Use this setting to measure the TX jitter. Set the **Measurement CDR bandwidth** option to **Datarate/1667** or **SIV_low**. Using the **SIV_low** setting is the same as if the **Stratix IV GX RX CDR BW** option is set to low. This setting depends on the protocol specification. Use **Datarate/1667** if the protocol calls for this transmitter jitter transfer bandwidth; otherwise, use **SIV_Low**.

Step 3: TX Subsystem Setup

Configure the TX settings. You can select **Stratix IV GX**, **Stratix IV GT**, or **Custom** for the TX subsystem configuration.

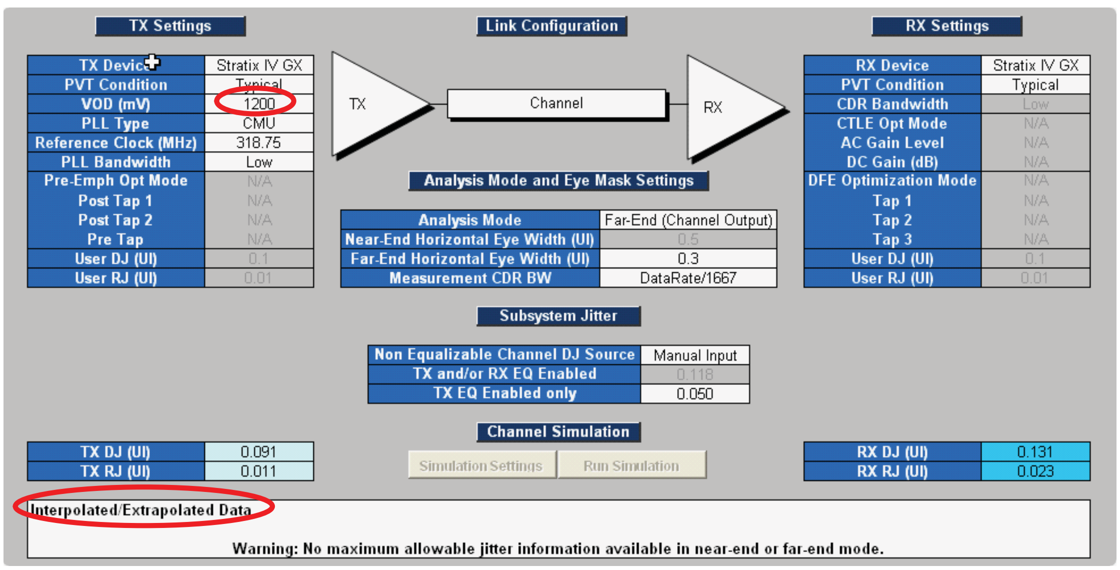
- Stratix IV GX or Stratix IV GT Device—if you select one of these, you must select the TX measurement conditions. Setting the TX parameters automatically populates the TX subsystem jitter values. The TX subsystem jitter values depend on the **Measurement CDR bandwidth** setting.
- PVT Condition—set the PVT condition to either **slow** or **typical**. Table 1–1 lists the temperature and voltage settings.

Table 1–1. PVT Condition

PVT Condition (Process)	Voltage	Temperature
Slow	-5%	100°C
Typical	Nominal	25°C

- VOD (mV)—Select the VOD setting from the **VOD (mV)** option drop down menu. Measured data is available for VOD at 400 mV and 1000 mV. For other VOD settings, the tool interpolates and/or extrapolates the TX deterministic jitter and TX random jitter values. If you use interpolation or extrapolation, the tool indicates the method used in the message bar, as shown in Figure 1–8. Interpolation is used when you set the **VOD (mV)** option to **600**, **700**, **800**, or **900** mV. Interpolation and/or extrapolation is used when you set the **VOD (mV)** option to **200** or **1200** mV.

Figure 1–8. Warning Message when the TX Subsystem Jitter is Interpolated or Extrapolated



- PLL Type—Stratix IV GX and GT devices have two types of transmitter phase-locked loops (PLLs), advanced technology extended (ATX) (also known as LC) and clock multiplier unit (CMU) (ring oscillator). The ATX PLL provides lower jitter, but is limited to a narrow frequency band.
  - Reference Clock (MHz)—select the PLL input reference clock frequency from the **Reference Clock (MHz)** drop down menu. If the measurement data is not available for the selected data rate, the tool provides interpolated data. When interpolation is used, the tool ignores the reference clock parameter and this value is grayed out.
  - PLL Bandwidth—set the **PLL Bandwidth** option to either **Low** or **Medium**.

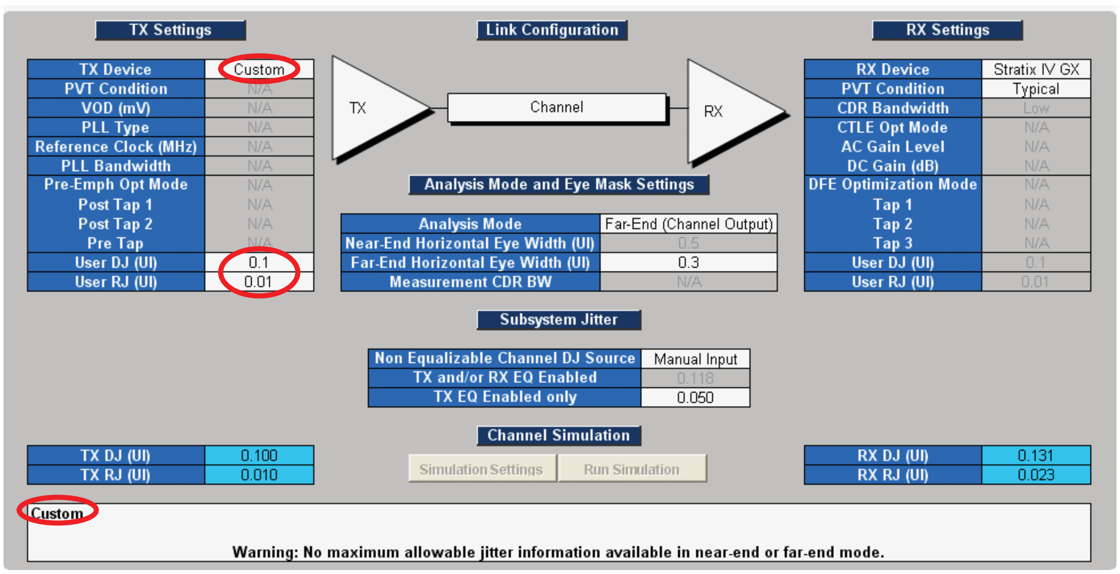
The pre-emphasis optimization mode and pre-emphasis tap settings (**Pre-Emph Opt Mode**) options are used by the integrated link simulator to estimate the non-equalizable channel deterministic jitter value in full-link and far-end modes.

For more information about pre-emphasis, refer to the FPGAs at 40 nm and > 10 Gbps: Jitter-, Signal Integrity-, Power-, and Process-Optimized Tarnsceivers white paper.

- Custom Device—if you selected **Custom** for the **TX Device** option, you must specify the TX **User DJ (UI)** and **User RJ (UI)** values. You must obtain these values from the appropriate source. You can chose **Custom** to investigate various "what-if" scenarios. Figure 1–9 shows an example of the link configuration using **Custom** for the TX device.

  Either TX or RX must be an Altera Stratix IV GX or GT device.

Figure 1–9. Link Configuration for a Custom TX



Step 4: RX Subsystem Setup

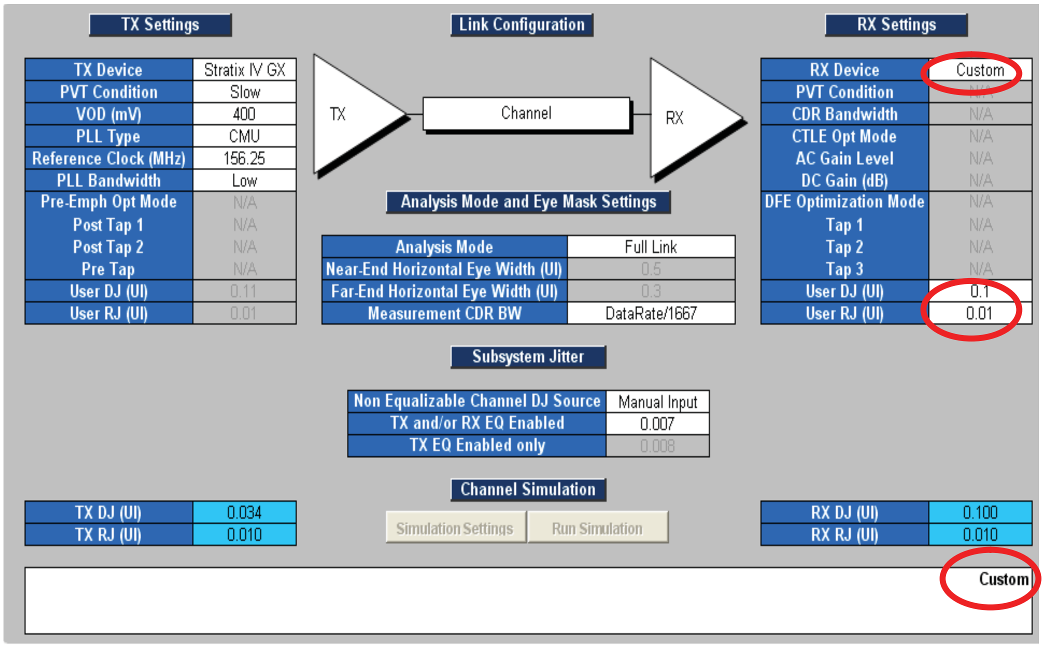
Configure the RX settings. You can select **Stratix IV GX**, **Stratix IV GT**, or **Custom** for the RX subsystem configuration.

For the PVT condition, refer to Table 1–1 on page 1–10.

- Stratix IV GX or Stratix IV GT Device—if you select either **Stratix IV GX** or **Stratix IV GT** for the RX, also select the PVT condition from the **PVT Condition** drop down menu. Choosing the RX as **Stratix IV GX** or **Stratix IV GT** automatically populates the RX subsystem jitter parameters.
- Custom Device—if you select **Custom** for the RX type, you must also specify the RX **User DJ (UI)** and **User RJ (UI)** values. Figure 1–10 shows an example of the link configuration for a **Custom** RX device. You can select **Custom** to investigate various "what-if" scenarios.

  Either TX or RX must be an Altera Stratix IV GX or GT device.

Figure 1–10. Link Configuration for a Custom RX



The continuous time linear equalizer (CTLE) optimization mode (**CTLE Opt Mode**), **AC Gain Level**, **DC Gain Level**, **DFE Optimization Mode** (including the decision feedback equalization tap settings options) are used by the integrated link simulator to estimate the non-equalizable channel deterministic jitter value in full-link and far-end mode.

For more information about the continuous time linear equalizer (AC gain and DC gain) and decision feedback equalization, refer to the FPGAs at 40 nm and > 10 Gbps: Jitter-, Signal Integrity-, Power-, and Process-Optimized Tarnsceivers white paper.

If you are using a custom device, you must find a method to solve for the non-equalizable channel DJ.

Step 5: Channel Subsystem Setup

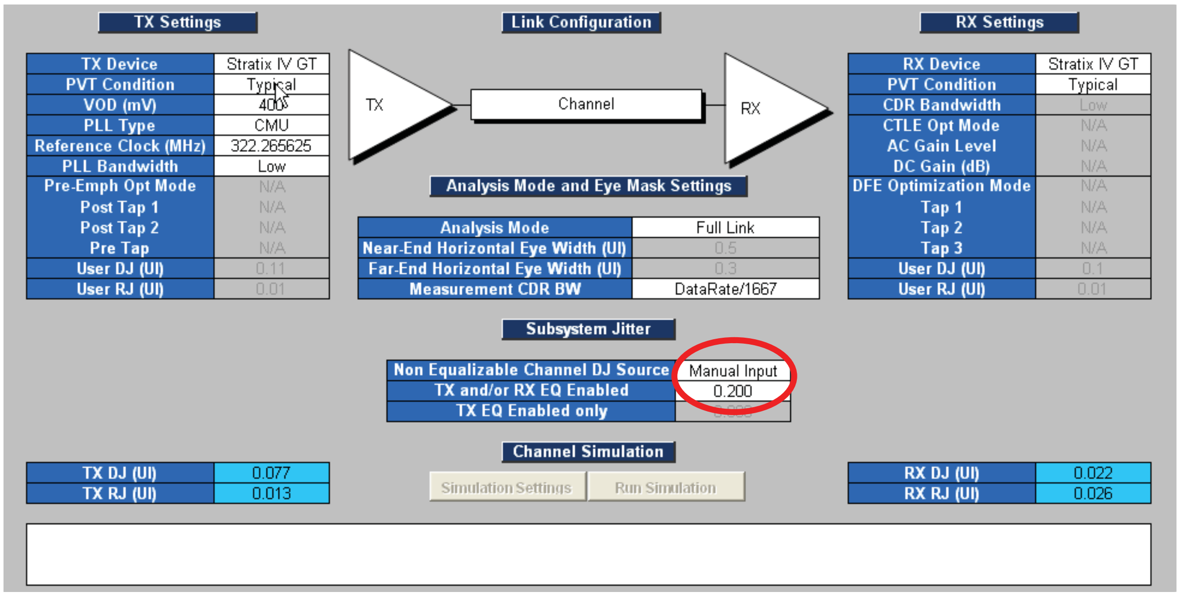
In full-link and far-end modes, you can either use the integrated link simulator to estimate the non-equalizable channel deterministic jitter or manually enter the value. Based on the analysis mode and non-equalizable channel deterministic jitter estimation method you selected, the appropriate box is enabled.

Non-Equalizable Channel Deterministic Jitter in Full-Link or Far-End Modes

Non-equalizable channel deterministic jitter is defined as channel jitter (intersymbol interference [ISI] and/or crosstalk) that cannot be compensated by using TX pre-emphasis and/or RX equalizations. In full-link and far-end modes, you can either manually enter the non-equalizable channel deterministic jitter value or use the link simulator to estimate the non-equalizable channel deterministic jitter value.

In manual mode, you must enter either the **TX and/or RX EQ Enabled** or **TX EQ Enabled only**, as shown in Figure 1–11.

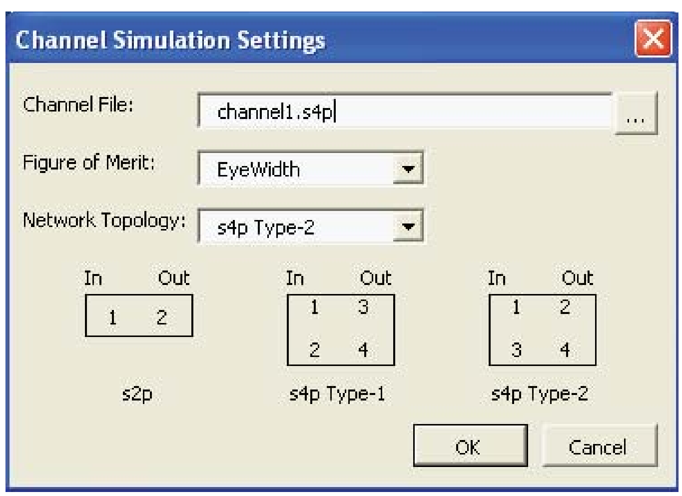
Figure 1–11. Manually Entered Non-Equalizable Channel Deterministic Jitter



In simulation mode, you must provide the channel information and select either **Manual** or **Automatic** for the mode of optimization for the **Pre-Emphasis Opt Mode**, continuous time linear equalizer (**CTLE Opt Mode**), and decision feedback equalization (**DFE Optimization Mode**) options.

- **Channel Simulation Settings**—click **Simulations Settings** under **Channel Simulation** to open the **Channel Simulation Settings** dialog box (Figure 1–12).

Figure 1–12. Channel Simulation Settings



The **Channel Simulation Settings** options are as follows:

- **Channel File**—provides the path to the channel S-parameters files in touchstone format. If the S-parameters file is not in the same location as the HST jitter and BER estimator spreadsheet tool, they are copied to the tool folder. This channel file must account for all the discontinuities due to the PCB traces, vias, connectors, and/or backplanes.
- **Figure of Merit**—choose the **EyeWidth**, **EyeHeight**, or **EyeArea** optimization method from the drop-down menu. Use this option to optimize the pre-emphasis and/or equalization settings in auto mode.
- **Network Topology**—specify the S-parameters type and port mapping used to generate the S-parameters file.

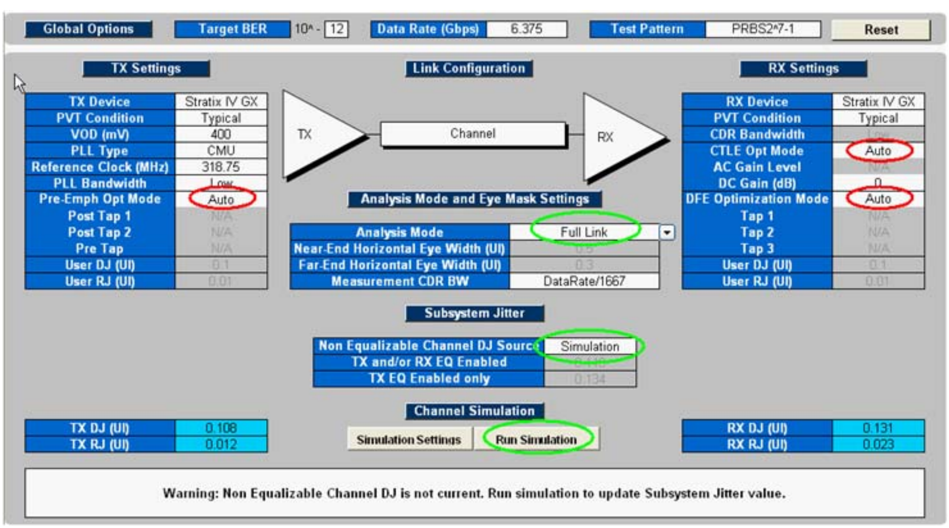
  Type 1: If ports 1 and 2 are inputs and 3 and 4 are outputs.

  Type 2: If ports 1 and 3 are inputs and 2 and 4 are outputs.

  Use an S-parameters data viewer to identify S-parameters port mapping. If the S12 channel loss increases as the data rate increases, use Type 2; otherwise, use Type 1.

- Channel Equalization Optimization Mode—select **Manual** or **Auto** mode of optimization for pre-emphasis (**Pre-Emph Opt Mode**), continuous time linear equalizer (**CTLE Opt Mode**), and decision feedback equalization (**DFE Optimization Mode**). For the decision feedback equalization, in addition to **Manual** and **Auto**, there is a **Disable** option to bypass the decision feedback equalization. In manual mode, you must enter the settings to estimate the non-equalizable channel deterministic jitter. In auto mode, the simulator chooses the optimum settings to compensate for channel loss (Figure 1–13).

Figure 1–13. Run Simulation to Estimate Non-Equalizable Channel Deterministic Jitter in Full-Link Mode



- **Pre-Emph Opt Mode**—in manual mode, the pre-emphasis settings available are **Pre-tap (-15 to 15)**, **1st post-tap (0 to 31)**, and **2nd post-tap (-15 to 15)**.

  ☞ A valid pre-emphasis setting depends on the data rate and VOD.

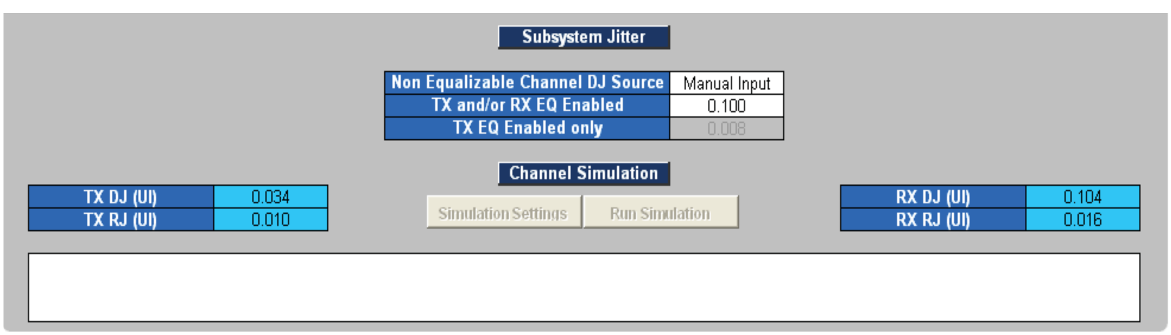
- **CTLE Opt Mode**—in manual mode, set the **AC Gain Level** option between 0 and 15, and set the **DC Gain Level** option to **0 (0 dB)**, **1 (3 dB)**, **2 (6 dB)**, **3 (9 dB)**, or **4 (12 dB)**. In auto mode, set the **AC Gain Level** option to **Auto** and for the **DC Gain Level** option, choose one of the following (in **DC Gain Level**—continuous time linear equalizer in auto mode):
  - **0**—DC gain is set to 0 dB.
  - **0/1**—selects an optimum value between 0 and 3 dB
  - **0/1/2**—selects an optimum value between 0, 3, and 6 dB
  - **0/1/2/3**—selects an optimum value between 0, 3, 6, and 9 dB
  - **0/1/2/3/4**—selects an optimum value between 0, 3, 6, 9, and 12 dB
- **DFE Optimization Mode**—in manual mode, the decision feedback equalization settings are **Tap1 (0 to 7)**, **Tap2 (-7 to 7)**, and **Tap3 (-7 to 7)**. Set the **DFE Optimization Mode** option to **Auto** mode to have the simulator pick the optimum values. Set the **DFE Optimization Mode** option to **Disable** to bypass the decision feedback equalization engine.

Click **Run Simulation** to run the simulator and update the **TX and/or RX EQ Enabled** option.

Subsystem Jitter

The **TX DJ (UI)**, **TX RJ (UI)**, **RX DJ (UI)**, and **RX RJ (UI)** subsystem jitter fields are used only for displaying values. These values are measured or interpolated and/or estrapolated for Stratix IV GX and GT devices or the copies of the user-specified values for a Custom device. If the data displayed is interpolated or extrapolated, the message bar displays this information. The **TX and/or RX EQ Enabled** and **TX EQ Enabled only** options are used for both input and display. Figure 1–14 shows the subsystem jitter fields.

Figure 1–14. Subsystem Jitter

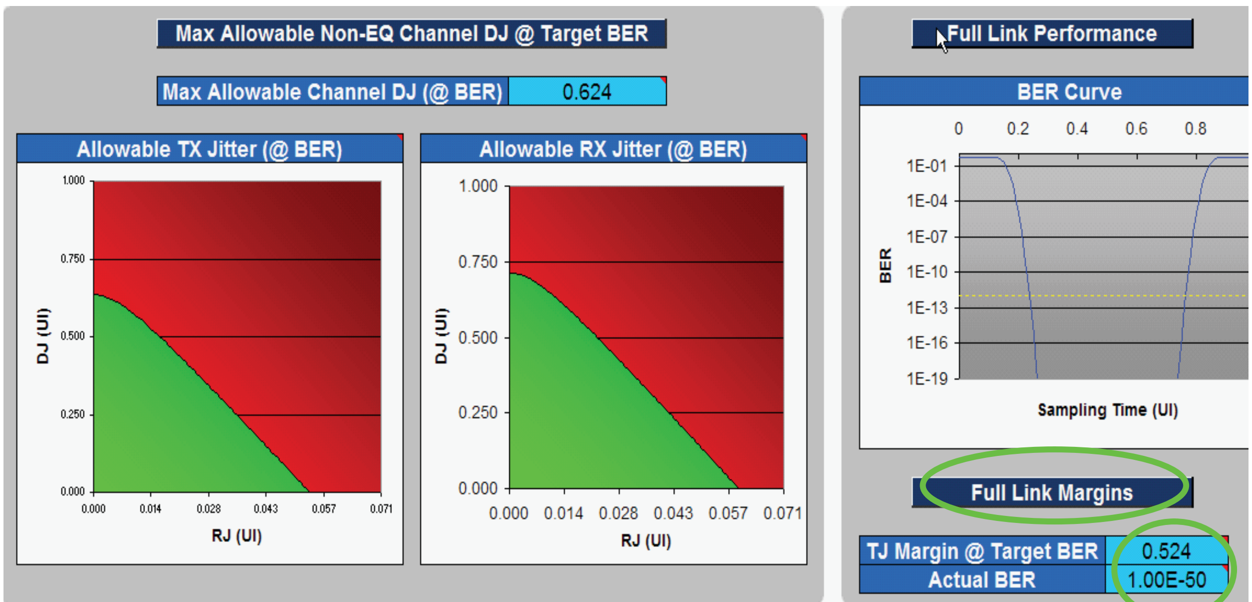


Step 6: Results

Interpret the link performance analysis results.

Figure 1–15 shows sample of the HST jitter and BER estimator tool analysis results. The allowable TX jitter, allowable RX jitter, and the maximum allowable non-equalizable channel deterministic jitter results are shown on the left side. The BER bathtub curve, TJ margin at Target BER, and actual BER results are shown on the right side. The allowable subsystems' jitter is not calculated if you select either far-end or near-end mode.

Figure 1–15. Full-Link Analysis Mode Results



☞ When considering the allowable TX and RX jitter, the plots provide the allowable margins for the random jitter and deterministic jitter to keep the BER performance in the green region.

Full-Link Results

TX jitter, RX jitter, channel jitter, and/or BER are essential for quantifying link performance. As Table 1–2 shows, any one of these can be estimated if the other three characteristics are known.

Table 1–2 lists the four scenarios of the analysis results shown in Figure 1–15.

Table 1–2. Analysis in Full-Link Mode *(Note 1)*

	TX	CH	RX	BER
Case 1—Link BER Estimation	✓	✓	✓	?
Case 2—Maximum Allowable Channel Deterministic Jitter Estimation	✓	?	✓	✓
Case 3—Allowable TX Jitter Estimation	?	✓	✓	✓
Case 4—Allowable RX Jitter Estimation	✓	✓	?	✓

Note to Table 1–2:

(1) ✓ = known characteristics; ? = to be estimated from the known information.

Case 1—Link BER Estimation

When you know the deterministic jitter and random jitter values of all the link components (for example, TX, RX, and channel), you can estimate the BER of this link. Three pieces of information, bathtub curve, TJ margin at the target BER, and actual BER are provided.

Case 2—Maximum Allowable Channel Deterministic Jitter Estimation

For a given (or chosen) TX and RX (for example, knowing their deterministic jitter and random jitter values) and target BER, you can find out how much non-equalizable chananel deterministic jitter is allowed for the link.

Case 3—Allowable TX Jitter Estimation

For a given (or chosen) RX deterministic jitter and random jitter, channel deterministic jitter, and target BER, you can find out how much deterministic jitter and random jitter is allowed for the TX. Because larger random jitter is allowed when deterministic jitter is smaller and vice versa, allowable TX deterministic jitter and random jitter is not a unique pair of values but any pair of values in the green region shown in Figure 1–15.

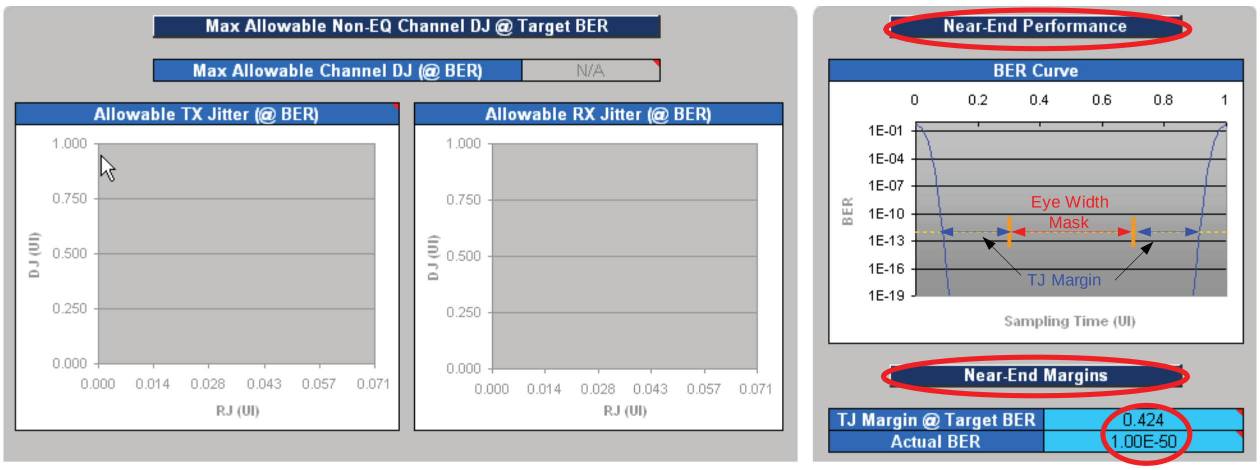
Case 4—Allowable RX Jitter Estimation

For a given (or chosen) TX deterministic jitter and random jitter, channel deterministic jitter, and target BER, you can find out how much deterministic jitter and random jitter is allowed for the RX. Because larger random jitter is allowed when deterministic jitter is smaller and vice versa, allowable RX deterministic jitter and random jitter is not a unique pair of values but any pair of values in the green region shown in Figure 1–15.

Near-End Results

Many high-speed standards (for example, PCI Express® [PCIe], Gigabit Ethernet [GbE], and Fibre Channel [FC]) require that a near-end mark be met at the TX output (for example, the horizontal eye opening at certain data rates must be larger than the specified value per the mask). In Figure 1–16, the orange bar represents the horizontal eye mask requirement. The Near-End Margin section describes the available horizontal eye opening margin to the eye mask at the target data rate, as well as the estimated achievable BER.

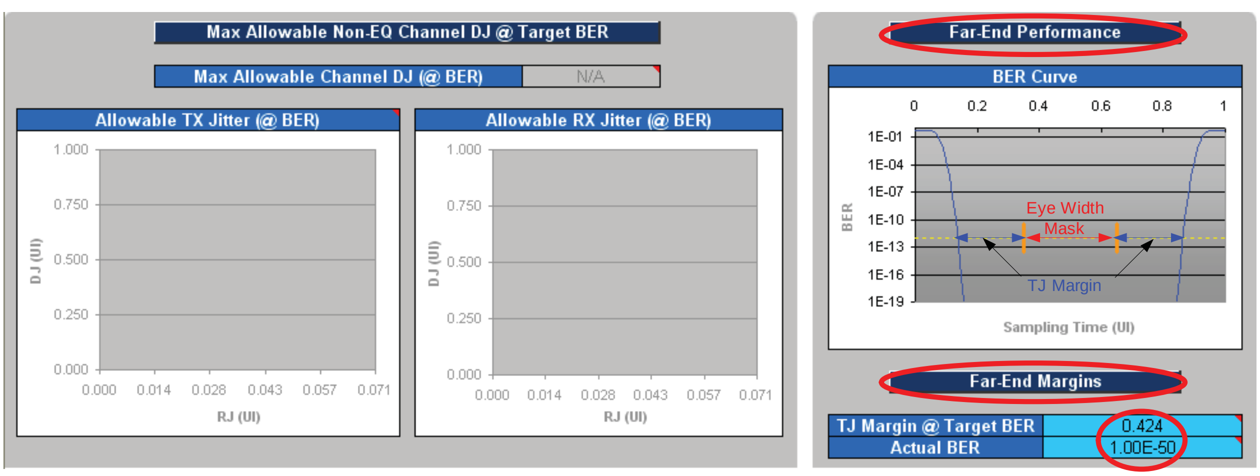
Figure 1–16. Near-End Analysis Mode Results



Far-End Results

Many high-speed standards (for example, PCIe, GbE, and FC) require that a far-end mask be met at the RX input (for example, the horizontal eye opening at certain data rates must be larger than the specified value per the mask). In Figure 1–17, the orange bars represent the horizontal eye mask requirement. The Far-End Margin section describes the available horizontal eye opening margin to the eye mask at the target data rate, as well as the estimated achievable BER.

Figure 1–17. Far-End Analysis Mode Results



Summary

You can estimate the BER and TJ margin at the target BER of the link system if you know all the jitter components of the subsystems. In full-link mode, you can also estimate the allowable TX deterministic jitter and corresponding random jitter values, allowable RX deterministic jitter and corresponding random jitter values, and the maximum allowable channel deterministic jitter value. The HST jitter and BER estimator tool allows you to quickly identify if a particular device meets your BER requirement based on the link subsystems' jitter.

2. Additional Information

Document Revision History

The table below displays the revision history for the chapters in this User Guide.

Date	Document Version	Changes Made
July 2010	1.0	Initial release.

How to Contact Altera

For the most up-to-date information about Altera® products, refer to the following table.

Contact *(1)*	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Non-technical support (General)	Email	nacomp@altera.com
Non-technical support (Software Licensing	Email	authorization@altera.com

Note to table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, file names, file name extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design*.
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input`. Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
☞	The hand points to information that requires special attention.
CAUTION	A caution calls attention to a condition or possible situation that can damage or destroy the product or the user's work.
WARNING	A warning calls attention to a condition or possible situation that can cause injury to the user.
↵	The angled arrow indicates you should press the Enter key.
(feet icon)	The feet direct you to more information on a particular topic.