

5.0-Volt Tolerance in APEX 20KE Devices

Introduction

Technological advancements in deeper submicron processes have lowered the supply voltage levels of semiconductor devices, creating a design environment where system board devices may potentially use many different supply voltages, which can ultimately lead to voltage conflicts. To accommodate interfacing with a variety of devices on system boards, Altera® APEX™ 20KE devices have MultiVolt™ I/O interfaces that allow devices in a mixed-voltage design environment to communicate directly with APEX 20KE devices.

While the APEX 20KE device core has a supply voltage of 1.8 V, eight distinct banks of I/O pins can be independently powered by supply voltages of 1.8 V, 2.5 V, or 3.3 V, allowing APEX 20KE devices to interface with devices powered at these voltage levels. Additionally, slightly modifying the external circuitry allows 5.0-V tolerance for the APEX 20KE I/O pins.

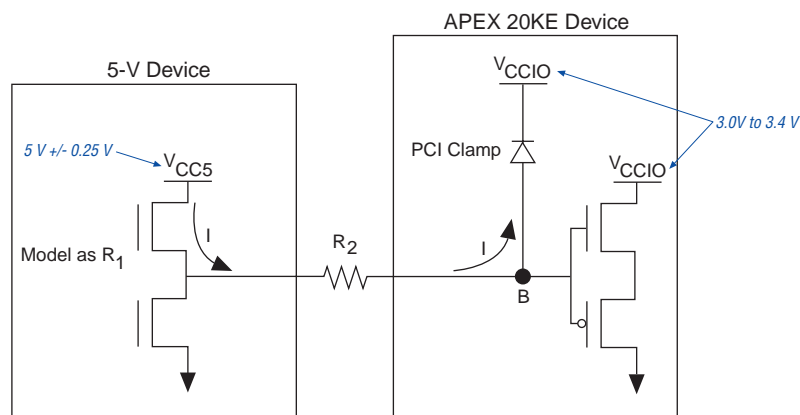
This white paper discusses how to drive an I/O, a dedicated clock, or a dedicated fast I/O pin in APEX 20KE devices with 5.0-V signals.

APEX 20KE Devices

The VCCINT pins on APEX 20KE devices are connected to 1.8 V. The VCCIO pins can be connected to 1.8 V, 2.5 V or 3.3 V. To interface with a 5.0-V device, the VCCIO pins need to be connected to 3.3 V. The output high voltage (V_{OH}) meets the 5.0-V transistor-to-transistor logic (TTL) high-level minimum of 2.4 V; therefore, APEX 20KE devices can drive 5.0-V TTL devices.

Because APEX 20KE devices are 3.3-V, 64-bit, 66 MHz PCI compliant, the input circuitry accepts a maximum high-level input voltage (V_{IH}) of 4.1 V. To have a 5.0-V powered device drive APEX 20KE devices, you must connect a resistor (R_2) between the APEX 20KE device and the 5.0-V device, as illustrated in [Figure 1](#).

Figure 1. APEX 20KE Interface with 5-Volt Devices



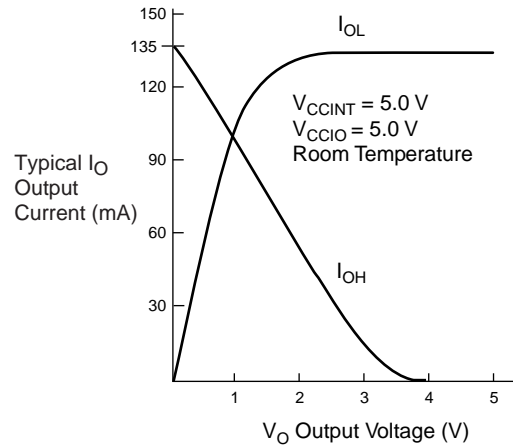
With the PCI clamping diode enabled and V_{CCIO} between 3.0 V and 3.4 V, the voltage at point B in [Figure 1](#) is 4.1 V or less. To limit large current draw from the 5.0-V device, R_2 should be small enough for a fast signal rise time and large enough so that it does not violate the high-level output current (I_{OH}) specifications of the devices driving the trace. The PCI Clamp in APEX 20KE devices can support at least 25 mA when voltage at point B (V_{IN}) - V_{CCIO} = 1.0 V (as specified in the *PCI Local Bus Specification, Revision 2.2*).

To compute the required value of R_2 , first calculate the model of the pull-up transistors on the 5.0-V driving device. This output transistor can be modeled as a resistor (R_1). To compute R_1 , divide the supply voltage (V_{CC5}) by the I_{OH}

as in the following equation: $R_1 = \frac{V_{CC5}}{I_{OH}}$

Refer to the specific 5.0-V device's data sheet for its output drive characteristics. Figure 2 shows an example of the typical output drive characteristics of a 5.0-V device.

Figure 2. Example Output Drive Characteristics of a 5.0-V Device



For the device in Figure 2, $R_1 = \frac{5.0V}{135mA}$. Because data sheet values are shown at typical conditions, subtract 20% from the data sheet value for guard band. This subtraction applied to the above example gives R_1 a value of 30 Ω .

R_2 should be chosen so as not to violate the I_{OH} specification of the driving device. Consider a device where the maximum $I_{OH} = 8$ mA. Due to the PCI Clamp, $V_{IN} = V_{CCIO} + 0.7$ V. The minimum $V_{IN} = 3.0$ V + 0.7 V = 3.7 V. The maximum V_{CC5} of the 5.0-V device = 5.25 V. Therefore, to compute R_2 , use the following equation:

$$R_2 = \frac{(5.25V - 3.7V) - (8mA \times 30\Omega)}{8mA} = 164\Omega$$

This analysis employs worst-case conditions. If your system will not see a wide variation in voltage supply levels, you may adjust accordingly.

Quartus Implementation

To interface APEX 20KE devices with 5.0-V devices, the optional PCI Clamp in the APEX 20KE I/O Element must be enabled. To enable the PCI clamping diode, go to the Quartus software's **Assignment Organizer** (Tools Menu) dialog box, click **Options for Individual Nodes & Entities**, and set the PCI I/O logic option to **ON**.

Hot-Socketing

APEX 20KE devices are designed to support hot-socketing without special design requirements. Signals can be driven into APEX 20KE devices before and during power-up without damaging the device. In addition, APEX 20KE devices do not drive out during power-up.

However, do not drive 5.0-V signals into APEX 20KE devices before the device is configured because the PCI clamping diode is not activated until configuration is complete.

For details on hot-socketing, see *Application Note 107 (Using Altera Devices in Multiple-Voltage Systems)*.

Power Sequencing

APEX 20KE devices have been specifically designed to tolerate any possible power-up sequence. Therefore, the VCCIO and VCCINT power planes may be powered in any order.

See the *APEX 20KE Programmable Logic Devices Errata Sheet* for additional information.

Conclusion

APEX 20KE devices have MultiVolt I/O support, allowing 1.8-V, 2.5-V, and 3.3-V devices to interface directly with APEX 20KE devices without causing voltage conflicts. In addition, APEX 20KE devices can interface with 5.0-V devices by slightly modifying the external hardware interface and enabling PCI clamping diodes via the Quartus software.



101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
<http://www.altera.com>

Copyright © 2000 Altera Corporation. Altera, APEX, APEX 20KE, Quartus, and MultiVolt are trademarks and/or service marks of Altera Corporation in the United States and other countries. Other brands or products are trademarks of their respective holders. The specifications contained herein are subject to change without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services. All rights reserved.