

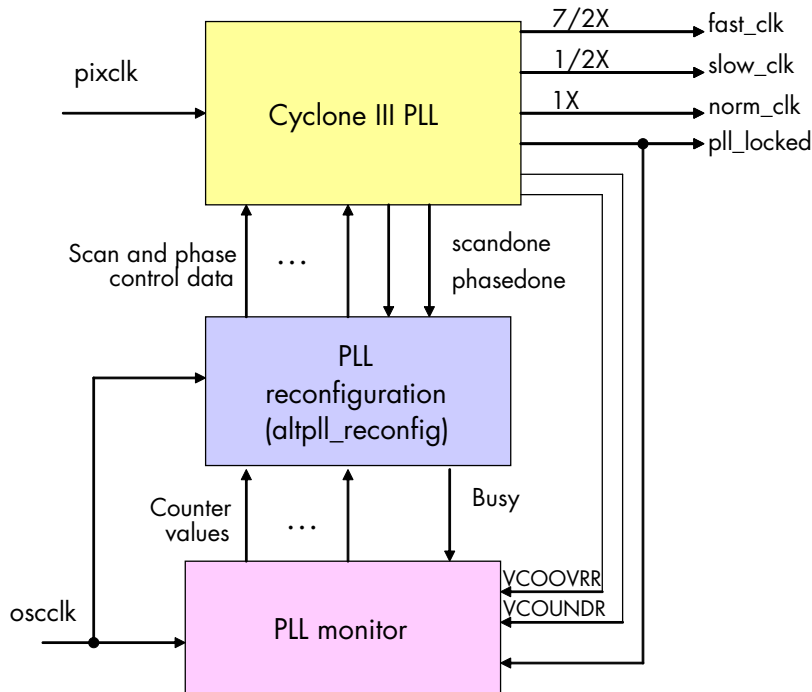


## Reference Design Building Blocks

Figure 2 shows a block diagram of the reference design. It consists of the following parts:

- PLL block
- PLL reconfiguration block
- PLL monitor block

Figure 2. Block Diagram of the Reference Design



### PLL Block

The PLL produces three output clocks that are multiples of the input frequency, `pixclk`:

- `fast_clk` = 3.5X `pixclk`
- `slow_clk` = 0.5X `pixclk`
- `norm_clk` = 1X `pixclk`

The lock signal is used to indicate if the PLL is able to acquire a lock after reconfiguring the PLL. The duty cycle of the output clock is set to 50 percent.

### PLL Reconfiguration Block

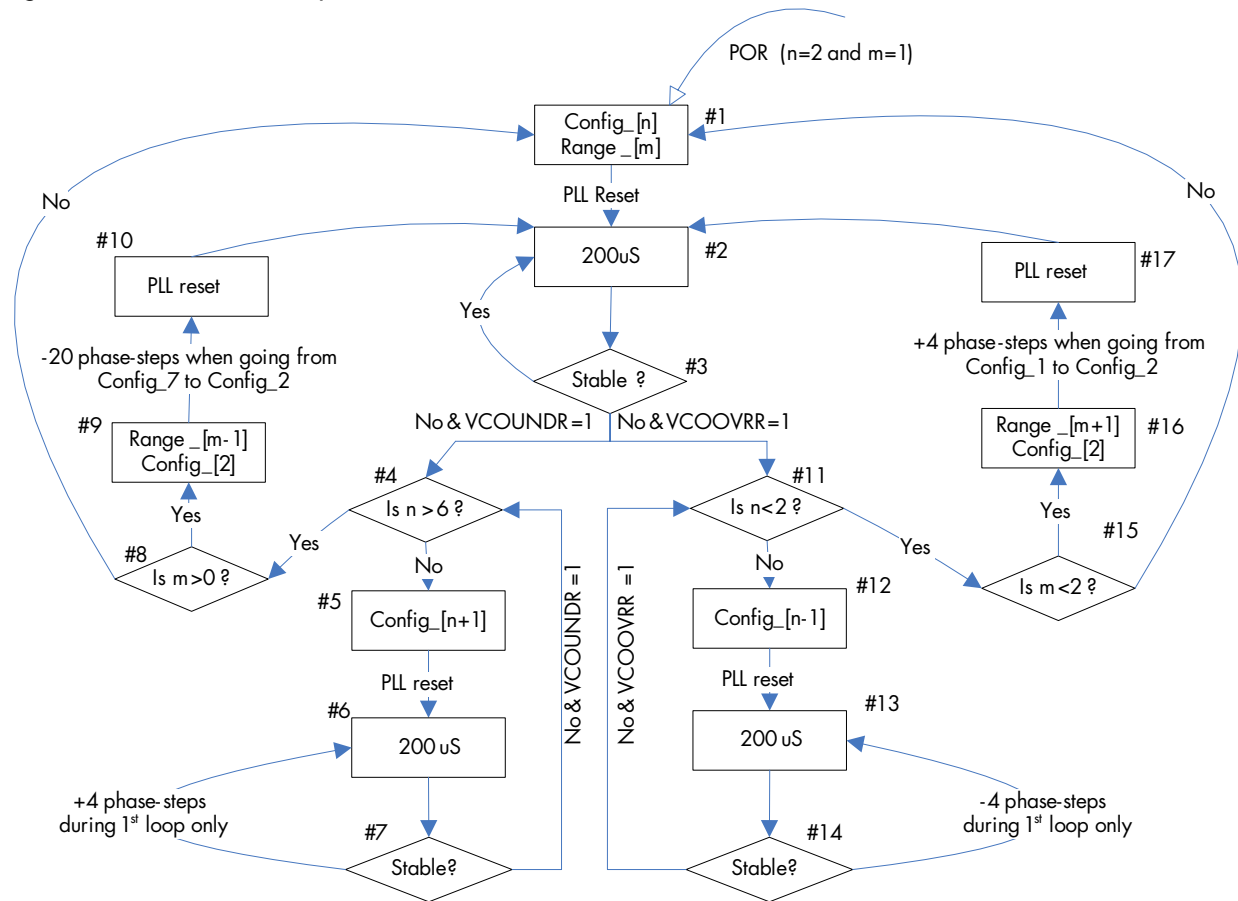
This block implements reconfiguration logic to facilitate dynamic real-time reconfiguration of the PLLs.

For more information on the PLL reconfiguration feature in Cyclone III FPGAs, refer to the *Cyclone III Handbook* and the *Phase-Locked Loops Reconfiguration (ALTPLL\_RECONFIG) Megafunction User Guide*.

### PLL Monitor Block

The PLL monitor block is the “heart” of the reference design. This block monitors the `VCOOVRR`, `VCOUNDR`, and lock signals to initiate real-time PLL reconfiguration in the state machine (shown in Figure 3).

Figure 3. State Machine Implemented in PLL Monitor Block



**Note:**

- (1) #x is the state number for easy reference.
- (2) PLL is stable after reconfiguration if (lock = 1) and (VCOVRR = 0) and (VCOUNDR = 0).

The entire input frequency range for this application (15 MHz to 135 MHz) is divided into sub-ranges, with the PLL configuration (M/N/C counter setting and the reference voltage for VCO range detector) for each sub-range stored in FPGA memory. The trip point for VCO range detector is programmable (see Table 1), and each setting corresponds to an optimum set of trip points for the reference design.

Table 1. VCO Range Detector Settings Used in the Reference Design

VCO Range	Reserved_3	Reserved_4	Reserved_6	Reserved_0
Range_0	0	0	1	1
Range_1(default)	0	0	1	0
Range_2	1	1	0	0



For more information on the location of the reserved bits in the PLL reconfiguration scan chain, refer to AN 507: Implementing PLL Reconfiguration in Cyclone III Devices.

If the input frequency to the PLL changes to a point where the VCOUNDR or VCOVRR is asserted, PLL reconfiguration is initiated to reconfigure the PLL with the next predetermined PLL configuration (as shown in Table 2). If a lock is not acquired with this configuration, the PLL is reconfigured again with the next higher sub-range configuration. This process repeats until the PLL acquires a lock after reconfiguration.

Table 2. PLL Configurations Used in the Reference Design

Configuration	Setting					
	N counter	M counter	Loop filter resistance	C0(1X)	C1(0.5X)	C2(3.5X)
Config_1	1	7	28	7	14	2
Config_2	1	14	27	14	28	4
Config_3	1	21	27	21	42	6
Config_4	1	28	27	28	56	8
Config_5	1	35	27	35	70	10
Config_6	1	42	27	42	84	12
Config_7	1	49	27	49	98	14

## Reference Design Testing

Altera has characterized the reference design and is confident that it works well with the following conditions:

- The initial input frequency is 60 MHz to 80 MHz, which can vary from 15 MHz to 135 MHz (both inclusive) in later stages.
- The input frequency is ramped monotonically with a maximum ramp rate of 27 MHz/ms.
- The total time taken for the PLL to acquire a lock after reconfiguration is less than 5 ms.



For more information about PLL timing specifications, refer to the *Cyclone III Device Datasheet: DC and Switching Characteristics* chapter in Volume 2 of the *Cyclone III Device Handbook*.

## Using the Reference Design

The unknown  $F_{REF}$  reference design can be downloaded from the Altera website at [www.altera.com/literature/wp/wp-01056-pll\\_reconfig.qar](http://www.altera.com/literature/wp/wp-01056-pll_reconfig.qar). To use the design example:

1. Restore the archived project (pll\_reconfig.qar).
2. Choose the correct device.
3. Make the pin assignments to the pins as listed in [Table 3](#).
4. Compile the project in the Quartus® II software (version 7.2 and above).

Table 3. List of Pins That Need User Assignments

Pin Name	Direction	Description
fast_clk	Output	PLL output clock, 3.5X pixclk
ip_busy	Output	IP status signal, active high
norm_clk	Output	PLL output clock, 1X pixclk
Oscclk	Input	Connects to the scnclk of the PLL reconfiguration port
Pixclk	Input	Input clock to PLL
pll_locked_ext	Output	PLL lock signal, active high
Rstn	Input	IP reset (Active low)
slow_clk	Output	PLL output clock, 0.5X pixclk
vcooverrange_ext	Output	Flag for indicating VCO over range (Active high)
vcounderrange_ext	Output	Flag for indicating VCO under range (Active high)

## Conclusion

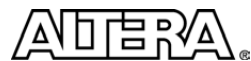
Cyclone III PLLs are now able to support “unknown”  $F_{REF}$  video applications in the display market with this soft IP that leverages improvements made in the PLL block. System designers can make use of this new functionality seamlessly, thus saving valuable engineering resources and getting to market faster.

## Further Information

- *Phase-Locked Loops Reconfiguration (ALTPLL\_RECONFIG) Megafunction User Guide:*  
[www.altera.com/literature/ug/ug\\_altpll\\_reconfig.pdf](http://www.altera.com/literature/ug/ug_altpll_reconfig.pdf)
- *AN 507: Implementing PLL Reconfiguration in Cyclone III Devices:*  
[www.altera.com/literature/an/AN507.pdf](http://www.altera.com/literature/an/AN507.pdf)
- *Cyclone III Device Handbook:*  
[www.altera.com/literature/lit-cyc3.jsp](http://www.altera.com/literature/lit-cyc3.jsp)
  - Volume 2, Section 1, Chapter 1: *Cyclone III Device Datasheet: DC and Switching Characteristics:*  
[www.altera.com/literature/hb/cyc3/cyc3\\_ciii52001.pdf](http://www.altera.com/literature/hb/cyc3/cyc3_ciii52001.pdf)

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