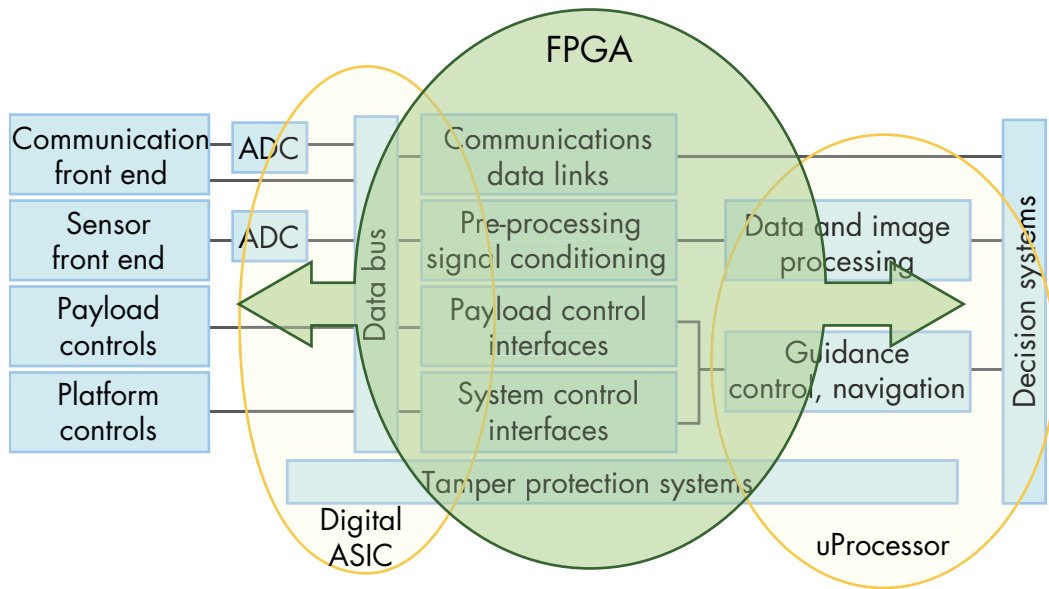


## 40-nm FPGAs and the Defense Electronic Design Organization

### Introduction

With Altera’s introduction of 40-nm FPGAs, the design domains of military electronics that can be addressed with programmable logic devices (PLDs) are growing (see [Figure 1](#)). This growth is a response to military integration requirements, as well as a function of the rising cost of new ASIC starts in successive generations of silicon geometry. Functions that were once restricted to ASIC designs or microprocessor systems now benefit from the shorter design cycle times and simpler hardware verification processes of an FPGA.

Figure 1. FPGAs Are Expanding in Technology Domain Applications in Military Electronics



*Source: Redrawn from Figure 12, “Report of Department of Defense Advisory Group on Electronic Devices - Special Technology Area Review on Field Programmable Gate Arrays (FPGAs) for Military Applications.” July 2005. Office of the Under Secretary of Defense, Acquisition, Technology, and Logistics. Cleared for Open Publication 23 August, 2005 by the Office of Freedom of Information. DTIC Accession Number ADA442913.*

Though FPGA-enabled functional integration leads to important efficiencies in military systems design, it also has a fundamental effect on the systems engineering process, as well as the management of engineering organizations in defense programs. Altera® FPGAs are causing system design roles to expand, affecting the mix of talent needed in engineering organizations, as well as their organizational structure.

### Military User Requirements

The relationship between military user requirements and commercially available technology is intentional. A growing number of national militaries are equipped entirely with commercial-off-the-shelf (COTS) equipment. Likewise, the U.S. military continually is challenged to leverage commercially available technology into battlefield settings. Today’s soldiers are used to handheld and wireless technology at home and demand similar soldier-to-soldier connectivity in the field.

One particular application example is next-generation airborne sensors. New, larger PLDs offer one of the best ways to integrate flexible circuitry for multiple modes in a productive design flow that allows for simple technical upgrades without reinventing critical intellectual property (IP).

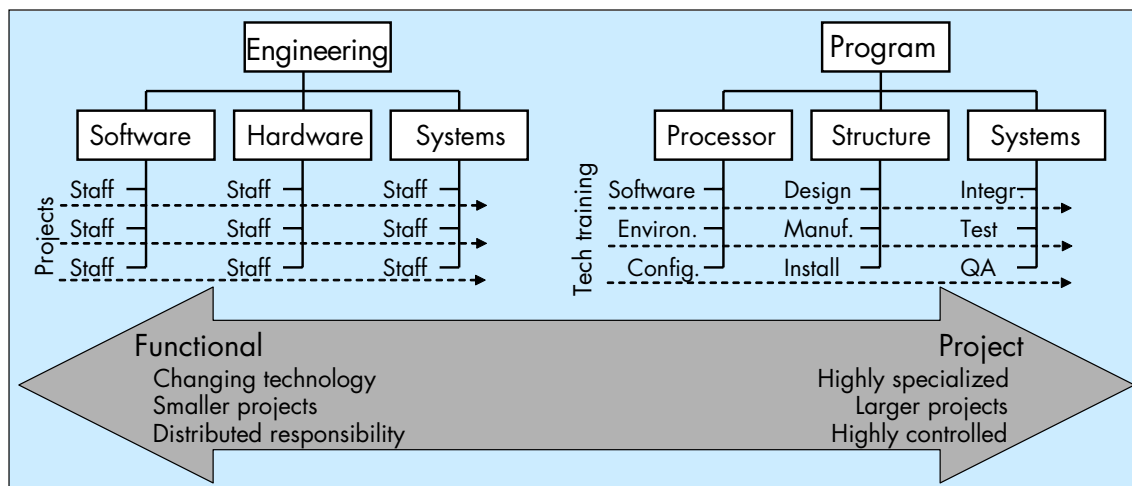
While the large number of technical requirements engaging systems engineers cannot be easily summarized, there are four very large initiatives in military electronics technology that are addressed by the larger class of new FPGAs. These are reductions in size, weight, and power (SWaP); common data bus standards (“open systems”); design re-use; and anti-tamper technologies.

The simplest approach to reducing SWaP is integrating many subsystems into a single chip. While this can be enabled through robust systems engineering processes and workflow controls, having multiple subsystems increases the importance of open systems design and anti-tamper technologies for FPGAs. In order to see improvements in efficiency in new larger “system-on-a-chip” (SOC) designs, design re-use must be an integral part of systems design flow.

## Engineering Organizational Structure

Historically, engineering organizations have been designed around one of two large classes: functional organizations and project organizations (see Figure 2). Most engineers and managers are familiar with the differences between these two classes. Functional organizations are built around engineering or sub-product engineering proficiencies, allowing for a focus on technology and engineering best practices. Project organizations, on the other hand, are built around a specific customer product so that engineering talent is focused on the specific needs of a customer. Both classes have their situational advantages and disadvantages.

Figure 2. Spectrum of Engineering Organizations: From Functional to Project



With a larger portion of a system encapsulated in FPGA logic, there are two effects that the new larger FPGAs have on functional engineering organizations. The first, predictably, is a higher demand for FPGA design engineers on staff, and possibly realignment in the engineering subdivisions. The second impact is to pull systems and architectural engineers into the FPGA design effort. This requires either a strong systems engineering capability within the hardware and firmware organization, or a systems engineering staff capable of understanding the complex and new capabilities of PLDs.

Project organizations are better suited for large re-engineering programs that take advantage of new 40-nm Stratix® IV FPGAs. Unfortunately, project organizations are less likely to be tracking new product releases and state-of-the-art programmable logic. Many times a project organization will rely on internal research and development (IRAD) or cross-project collaboration to achieve new technology insertion.

On the other hand, functional organizations are more likely to be technology focused and able to translate new technologies across multiple programs. However, these organizations may lack the necessary momentum to adopt new chip technologies. In both cases, some fundamental changes in the systems engineering functions may be needed

in order to take advantage of the SWaP and design efficiency advantages of design integration into larger Stratix IV FPGAs.

## FPGA System Design Approach Changes

Fundamentally, the principles of requirements engineering and test do not change when several subsystems are consolidated into larger Stratix IV FPGAs and then distributed among engineers. However, the lines between hardware and software become more blurred as the concept of design interfaces expands to include data boundaries within the FPGA. Just as systems engineering now includes code and mega-executable partitioning among software Integrated Product Team (IPT) members, it now also encompasses FPGA architecture and design. FPGA component selection, when using larger FPGAs, will be driven as much or more by system requirements than hardware requirements.

### *What Skills Are Needed?*

One of the most difficult skill sets to hire into a design organization today is FPGA design, where job descriptions include:

- Strong VHDL and Verilog design experience
- Embedded computing experience
- Digital test and debug (logic analyzer) experience
- DMA and memory interface experience
- Knowledge of Ethernet over SONET, 10 Gigabit Ethernet, Serial RapidIO®, PCI Express, etc.

How many of these skills really are necessary to develop FPGA designs? The answer, of course, is all of them, but these skills can now be distributed among a team rather than consolidated into one or a small number of FPGA-knowledgeable design staff.

As in software engineering, new skills are needed in FPGA architecture and design partitioning. These are systems engineering functions and should require only a subset of FPGA design engineering skills. One increasingly discussed trend in both commercial and defense electronics is design outsourcing for FPGAs. This allows defense sector companies to focus on core competencies and shift risk to outside engineering houses on important issues such as signal integrity on high-speed interfaces. Though this makes sense for some engineering design organizations, it does not negate the need for strong systems-level knowledge of FPGA capabilities, design partitioning, and SOC architecture development to back up the most important engineering decisions in an electronic system.

### *Who Will Train Them?*

Training is a difficult subject in high-technology defense companies. This is particularly true in project-based organizations, where training is an “off-the-grid” activity. The “half life” of technical training can be very short—sometimes less than the time needed to assess training program effectiveness. (Some technical professionals claim that over half of what an engineering graduate learns in college is obsolete within five years.)

It is less and less likely that engineering departments will be able to hire employees with exactly the FPGA design skills they need, especially when new devices have ASIC-level complexity and require team-based design. Application-level knowledge (signal processing, imaging, etc.) combined with the required FPGA design skills is even more scarce. These difficulties can best be addressed by allowing experienced systems engineers to participate in FPGA design by using new tools with usable abstraction layers. While many processing card developers offer abstracted “development kit” solutions for application markets, these development kits become less applicable to the wide range of user applications as new PLDs are introduced. Commonality in design entry must come from another source.

One source is vendor-developed FPGA system tools such as Altera’s Quartus® II design software, which integrates early design requirements such as timing, physical synthesis, floor planning, and logic lock into a single tool. This

allows knowledgeable systems engineers and design groups to take a more systematic approach to design, as well as a team-based approach that is essential to large FPGA use.

Defense engineering departments will continue to rely on universities, FPGA vendor-supplied training, or hiring for the FPGA-specific skills they need, as it is not likely that internal training for PLD-specific skills will be cost-effective. However, it will be increasingly important to develop a company-internal team-based design process with requisite training. This process should highlight the company-approved tool flows, requirements, test, and verification processes, and risk management procedures. By participating in a company-developed, team-based design training process, design engineers will have a better idea what additional vendor training they need to participate fully in their design programs.

### Designing the New Electronics Engineering Organization

Moving up the silicon manufacturing technology curve may not seem like a good reason for reorganization. However, the reason to move to larger devices should be based on integration efficiencies and design productivity, which may necessitate changes in design roles.

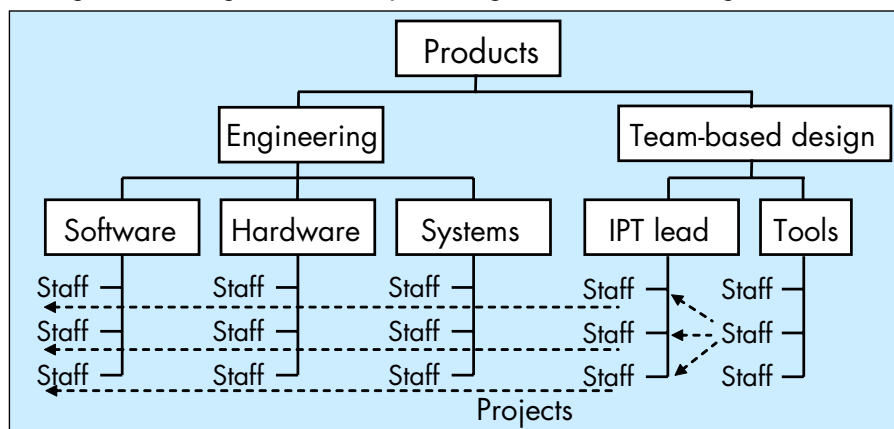
#### *Redefining Systems Engineering*

Systems engineering roles in defense systems companies have evolved over the years in many ways. Among the changes in scope are the inclusion of life-cycle management, design for cost and manufacturability, system of systems design, and open standards architectures (to include IP reuse). These are all derivatives of a team-based design methodology aimed at generating efficiencies elsewhere in the design lifecycle.

Cost drivers in defense electronics design—architecture, partitioning, verification, and board integration—are more strongly tied to design tool flow than ever before. With the potential for different vendors in each portion of the design flow, there is a great deal of risk to be managed by the engineering organization.

The fundamental structure of an organization should enable it to manage tool flow risk, as well as IP reuse throughout the organization. While there are many possible ways to tailor a design structure to defense company organizations, advocating a team-based design function controlled by a systems group or IP management staff is the most effective and efficient. In the example shown in [Figure 3](#), team-based design and tool flow are emphasized by placing all IPT managers within the team-based design group. The primary function of the IPT lead is to pursue a systems design using the best possible architecture given the current technology in tools and team-based design methodology.

Figure 3. Engineering Product Organization Emphasizing Team-Based Design



#### *Career Paths*

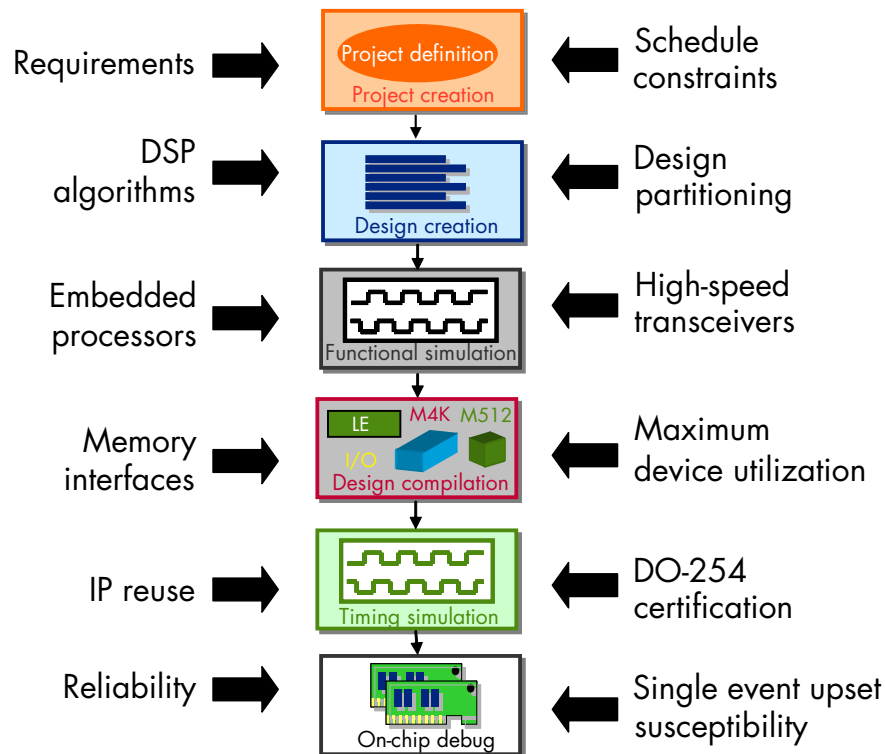
Creating a functional engineering organization should take into account three primary groups: company shareholders, customers, and employees. This means functional roles and skill divisions are articulated for both the best customer

product and the most efficient design process for shareholders. Just as important, however, is how the new organization establishes career paths and career development for the engineers that make up the organization. Because design flow methodology is such a critical technology and a cost driver for organizations that rely on PLD design, talent and project management potentials should be driven towards these competencies as (one) path for career advancement.

### Time to Focus on Design Flow

While there are many temptations to focus on the newest high-density and high-speed transceiver capabilities of the 40-nm Stratix IV FPGAs, military customers will necessarily want to focus their efforts on the impact of design-flow technology in their organizations (Figure 4).

Figure 4. Many of the Input Decisions in a Team-Based Design Tool Flow



Trade studies for device selection are traditionally cost versus performance. As FPGAs become more capable of containing a significant number of an electronic system's functions, the number-one systems cost driver is tool flow efficiency. While this is not simple to assess or measure, selecting the right tool flow for defense electronics design is paramount for cost competitiveness and efficient organizational operation.

### Conclusion

As with all new technologies, Stratix IV GX FPGAs should be evaluated not only by how they can be used in military electronics systems, but also by whether the organization can successfully implement the technology. In this white paper, we examined what hurdles may be necessary to implement large 40-nm designs: an organization that supports team-based design, engineer training, a systems engineering staff knowledgeable enough to redefine architectures around device integration opportunities, and a tool suite with designed-in productivity features and capabilities. Altera's Quartus II design software provides significant capabilities in compile time, design partitioning, and system interconnect in anticipation of this focus on design productivity. If your organization is looking for a way to reorganize around a team-based design methodology, please contact Altera to learn how to optimize your design flow to take advantage of 40-nm FPGAs.

## Further Information

- Altera's Military Risk and Productivity Management:  
[www.altera.com/products/devices/stratix-fpgas/stratix-iv/end-markets-applications/stxiv-military.html](http://www.altera.com/products/devices/stratix-fpgas/stratix-iv/end-markets-applications/stxiv-military.html)
- *Military Benefits of the Managed Risk Process at 40 nm*:  
[www.altera.com/literature/wp/wp-01063-military-benefits-managed-risk-process-40nm.pdf](http://www.altera.com/literature/wp/wp-01063-military-benefits-managed-risk-process-40nm.pdf)
- *Increasing Productivity With Quartus II Incremental Compile*:  
[www.altera.com/literature/wp/wp-01062-quartus-ii-increasing-productivity-incremental-compile.pdf](http://www.altera.com/literature/wp/wp-01062-quartus-ii-increasing-productivity-incremental-compile.pdf)
- *Comparing IP Integration Approaches for FPGA Implementation*:  
[www.altera.com/literature/wp/wp-01032.pdf](http://www.altera.com/literature/wp/wp-01032.pdf)
- Quartus II Design Software:  
[www.altera.com/products/software/sfw-index.jsp](http://www.altera.com/products/software/sfw-index.jsp)
- Increasing Productivity With SOPC Builder:  
[www.altera.com/products/software/products/sopc/sop-index.html](http://www.altera.com/products/software/products/sopc/sop-index.html)
- Altera's 40-nm Portfolio:  
[www.altera.com/b/40-nm-devices.html](http://www.altera.com/b/40-nm-devices.html)
- Contact the Altera sales team for more information:  
[www.altera.com/corporate/contact/con-index.html](http://www.altera.com/corporate/contact/con-index.html)

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