

## Understanding 40-nm FPGA Solutions for SATA/SAS

*This white paper describes the SATA and SAS protocols, how the protocols are used, explains the value SATA and SAS in terms of usage in an FPGA, and illustrates how Altera FPGAs can be used to develop a SATA or SAS solution.*

### Introduction

Serial ATA (SATA) and Serial Attached SCSI (SAS) are computer bus standards that have the primary function of transferring data (directly or otherwise) between the motherboard and mass storage devices (such as hard disk drives, optical drives, and solid-state disks) inside and outside the computer. These serial storage protocols offer several advantages over older parallel storage protocols (ATA and SCSI) interfaces:

- Faster data transfer
- Ability to remove or add devices while operating (hot swapping) (only when supported by operating system)
- Thinner cables for more efficient air cooling
- More reliable operation

Cables and connectors for SATA and SAS are interchangeable to a certain extent, in that a SATA storage device, cable, and connector can be used by a SAS host controller, but a SAS storage device and connectors cannot be used by a SATA host controller. This flexibility enables system designers the option of designing for SAS, a higher performance and higher cost solution, but using SATA as a lower cost option. Several versions of the SATA and SAS standards have been released so far, with each version primarily addressing the speed of a single data link. [Table 1](#) lists the released standards and their associated speeds.

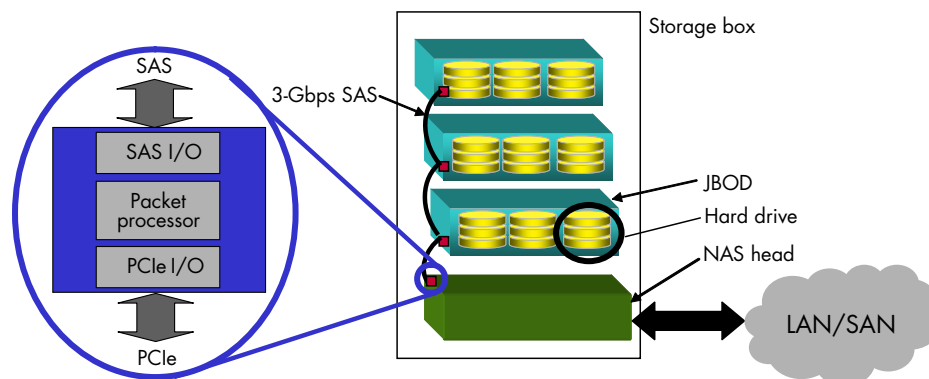
*Table 1. SATA/SAS Standards and Speeds*

SATA/SAS Standards	Speeds
SATA 1.0	1.5 Gbps
SATA 2.0, SAS 1.0	3 Gbps
SATA 3.0, SAS 2.0	6 Gbps

### Applications Using SAS and SATA

Because SATA and SAS are storage protocols, they are used as an interface to storage devices. Storage devices that use the SATA and SAS protocols are hard disk drives, optical drives, and solid-state disks. These storage devices reside in appliances like PCs, JBODs, disk arrays (SAN and NAS), multifunction printers, set-top boxes, and any other appliance that requires data to be stored for any length of time. [Figure 1](#) depicts a typical appliance in which SATA or SAS would be used.

*Figure 1. SAS Disk Array Example*



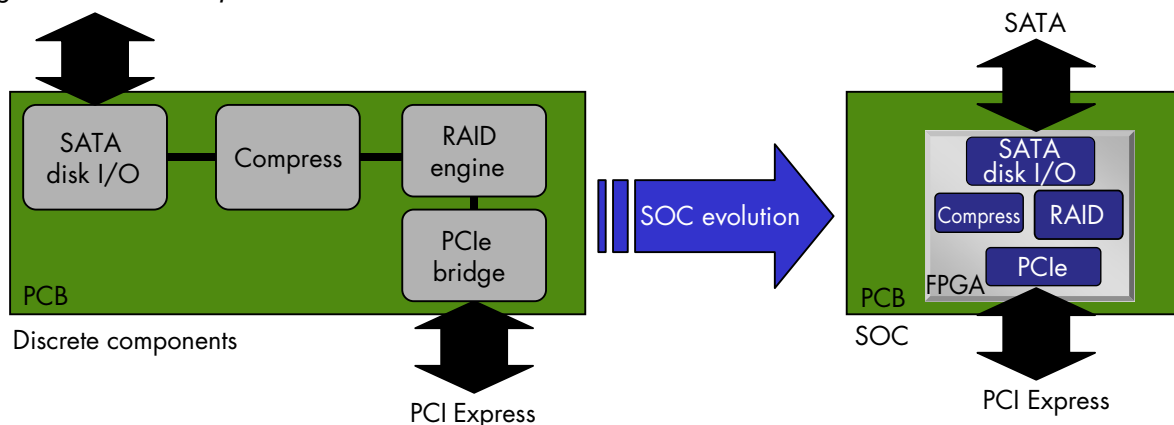
SATA is used in cost-sensitive applications, like PCs, set top boxes, SOHO storage enclosures, and other consumer-based applications. Designed as a replacement for ATA/IDE, this protocol predominantly is found in devices where low cost is essential.

In comparison, SAS is used in higher end systems, like SAN and NAS disk arrays, that are designed for high availability and little to no down time. These systems typically reside in data centers and provide five (5) nine's (9's) of availability, which means up-time 99.999% of the time. Applications needing this type of fault-tolerant storage are in the banking and stock trading industries. This type of reliability offered by SAS comes with a higher price tag, a justifiable return on investment when handling mission-critical data storage. SAS was designed as a replacement for SCSI, the protocol previously used for this type of storage.

## FPGA Use of SATA and SAS

Supporting a storage interface is just one of many different application needs to which an FPGA can conform. However, providing SATA and SAS storage interface is just one way an FPGA can be used in storage appliances. The FPGA also can bridge different protocols, such as bridging simple bus I/Os like PCI Express (PCIe) to SATA or SAS, or more exotically, bridging network interfaces such as Gigabit Ethernet (GbE), Fibre Channel, or SONET to SATA or SAS. In addition, an FPGA provides value-added functions to simple bridging applications, making the FPGA a system on chip (SOC). These value-added SOC functions include RAID, data compression, packet processing, and many more. By enabling development of SOC solutions, the FPGA simplifies system design, meaning that the FPGA reduces the need for multiple discrete devices by consolidating those functions in a single device. [Figure 2](#) demonstrates how an FPGA integrates functions to create an SOC for a RAID controller.

Figure 2. SOC Example

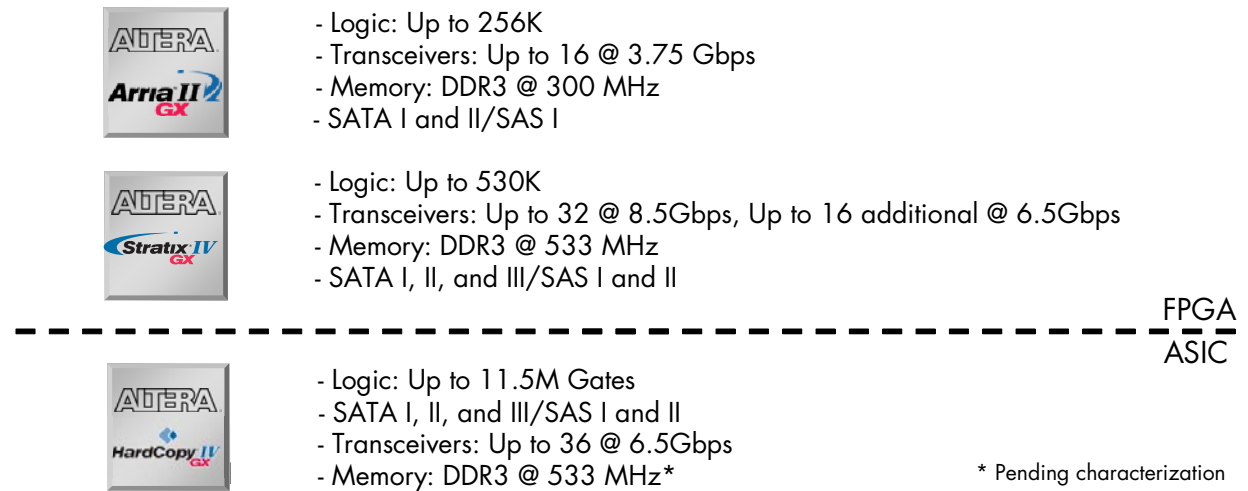


The FPGA offers an excellent platform on which to integrate many discrete ASIC or ASSP functions into a single chip solution. Now that Altera® FPGAs support SAS and SATA natively with the integrated transceivers, it is possible to leverage the integration option for storage applications.

## Altera SATA/SAS Solutions

Altera has developed SATA and SAS solutions based on their latest 40-nm Stratix® IV GX and Arria® II GX FPGAs with transceivers and 40-nm HardCopy® IV GX ASICs with transceivers. The Altera FPGAs and ASICs, coupled with SATA and SAS intellectual property (IP), offer a solution for developing storage interfaces on a single chip. This section describes which SATA and SAS standards are supported by Altera transceiver solutions, the electrical specification compliance of the transceivers ([Figure 3](#)), and the IP used for SATA and SAS.

Figure 3. Altera Hardware Support



### Altera Hardware Solution

The transceivers comply with the electrical standards for both SATA and SAS. Compliance to the electrical standards is accomplished using either built-in features in the transceiver block or with a small number of logic-based designs. Altera’s partner companies have several IP offerings that complete the SATA and SAS solutions, ranging from SATA 1 to SAS 2 in both host and device modes, which are summarized in [Table 2](#).

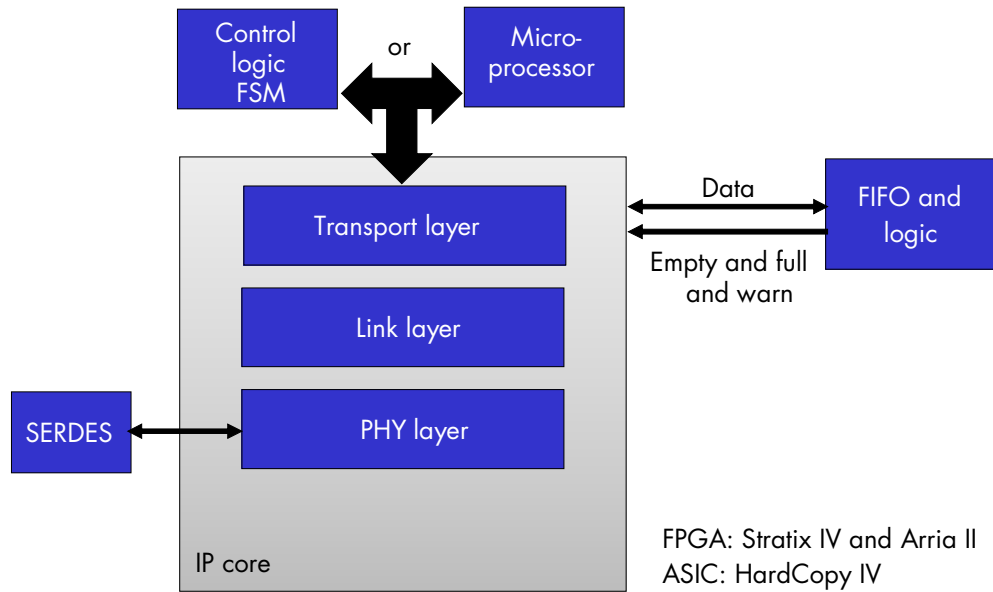
Table 2. Altera Hardware Compliance

SATA/SAS Specification	Arria II GX, Stratix IV GX, and HardCopy IV GX
Out of band signaling (OOB)	✓
Auto speed negotiation	✓
Rx/Tx electrical and jitter	✓
Spread spectrum clock (SSC)	✓
PPM tolerance	✓
Round-trip latency	✓
eSATA (cable)	✓

### SATA/SAS IP Solution

The IP portion of the Altera solution is core to the SATA and SAS I/O connectivity. The FPGA and ASIC provide the foundation, but the IP makes the SATA and SAS I/O possible. Altera has partners that have developed SATA and SAS IP for both host and device interfaces. As shown in [Figure 4](#), the IP core has all the basic components of a SATA and SAS interface: a physical layer interface that connects to the embedded transceivers, a link layer, and a transport layer. In addition, the IP core includes a processor interface that provides a pathway for a host system to monitor core and provide control instructions. The core uses the 8b/10b coding block, the DPRIO block, and the signal detect and electrical idle—all in the Altera transceivers—for protocol coding, speed negotiation, and out-of-band signaling.

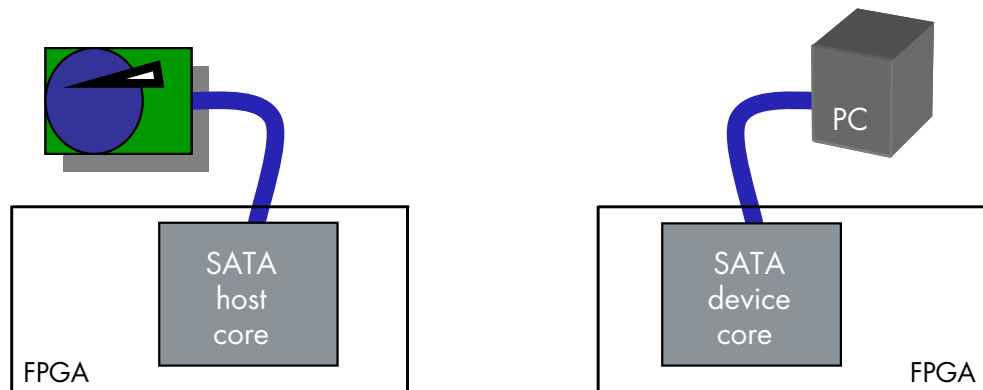
Figure 4. SATA/SAS IP Core



**Building a SATA and SAS Solution With IP and Altera Hardware**

A good way to demonstrate the capability of the Altera-based SATA and SAS solution is with a design that can test both host and target (device side) functions. This can be done in an FPGA by using a host or device IP core, a FPGA, and a host controller in a PC or disk drive. While SATA is used in Figure 5, either a SATA or SAS core may be used in the host or device designs. In the target design, the FPGA acts as a storage device for the host controller in the PC. In the host design, the FPGA performs host controller functions and stores data on the hard drive. The SATA host controller reads and writes data to and from the SATA hard disk drive, and a SATA target provides an endpoint storage interface for stored data to the PC.

Figure 5. Host (left) and Device (right) Design Examples



The FPGA and IP provide the foundation for SATA interface to both host and target devices, but more is needed. For a complete target (device) solution, a storage device like a hard drive or flash drive must be connected to the FPGA. A complete host solution needs application layer software added to the IP to enable data to be passed from one application to a storage device connected to the FPGA. Both the host design and target design are used for interoperability and industry compliance testing, as these allow both host and device functionality to be verified.

## Altera Development Platforms

For design validation testing, Altera uses the Stratix IV FPGA and a SATA/SAS I/O connector. A Stratix IV GX platform includes the Stratix IV GX signal integrity board (Figure 6) used in conjunction with an SMA to SATA paddle card for SATA I/O connectivity. This creates a hardware development platform for SATA/SAS testing. The hardware platform plus a soft SATA/SAS IP core can be used for functionality, specification-compliance, interoperability, and performance testing.

Figure 6. Stratix IV GX FPGA Platform

### Stratix IV GX signal integrity development kit

- EP4SGX230KF40
- 8 full duplex transceiver channels routed to SMAs

### SATA/SAS SMA paddle card

- SMA to female SATA/SAS connector
- Facilitates SATA/SAS compliance testing; connection to the SATA/SAS device



## Conclusion

Altera's 40-nm FPGAs and ASICs with transceivers provide an excellent way to develop SOC solutions for storage applications. The FPGA fabric enables system designers to integrate more functions in a single-chip solution, simplifying solution design and enabling integration of transceivers for SATA/SAS I/O connectivity. Altera's portfolio of 40-nm FPGAs and ASICs transceivers in combination with SATA/SAS IP cores creates a interface that can be used for a SATA/SAS solution.

## Further Information

- Serial ATA (SATA):  
[www.serialata.org](http://www.serialata.org)
- Serial Attached SCSI (SAS):  
[www.scsita.org](http://www.scsita.org)
- Literature: Arria II GX Devices:  
[www.altera.com/literature/lit-arria-ii-gx.jsp](http://www.altera.com/literature/lit-arria-ii-gx.jsp)
- Literature: Stratix IV Devices (E, GX, and GT variants):  
[www.altera.com/literature/lit-stratix-iv.jsp](http://www.altera.com/literature/lit-stratix-iv.jsp)

## Acknowledgements

- Bryce Mackin, Product Marketing Manager, I/O Solutions, High-End Product Marketing, Altera Corporation



101 Innovation Drive  
San Jose, CA 95134  
[www.altera.com](http://www.altera.com)

Copyright © 2009 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.