

Altera’s technology innovations in 20 nm devices will move customers’ designs up the silicon convergence continuum by providing them the ultimate system-integration platform to achieve unprecedented levels of performance, bandwidth, and power efficiency. These innovations will be delivered in a mixed-system fabric that brings together FPGA hardware and software flexibility along with the efficiencies of application-specific hard IP in a single device. Altera’s innovations in the mixed-system fabric are enabling customers to create differentiated system designs.

## Introduction

The primary challenge for designers and system architects today is to achieve dramatically higher bandwidth and higher performance while minimizing power consumption to meet overall thermal and cost requirements. To meet this challenge, solutions are needed that combine a mix of hardware performance, software programmability, hardened intellectual property (IP), software tool innovations, and the capability of 3D ICs. We call this blend a mixed-system fabric, the integration of microprocessors, digital signal processor (DSP) systems, FPGAs, ASSPs, and ASICs to merge into a single device. In this paper, we will show how these 20 nm technology innovations enable the mixed-system fabric and further extend silicon convergence. Through extending silicon convergence, Altera is enabling designers to create a measurable advantage in their systems.

## Product Development Challenges

The challenges of designers and system architects can be summarized as a set of constraints and market needs related to data throughput, processing performance, lower power, lower cost, lower and less risky development time, and feature differentiation. The order of importance in each of these categories varies by application and customer segment, but, nonetheless, every designer experiences some sort of constraint or competitive challenge in each of these categories (Figure 1).

**Figure 1. Common Constraints in Modern Electronic Design**



These challenges and constraints introduce designers to a variety of existing and emerging silicon processing technologies, including ASICs, ASSPs, microprocessors and multicore processors, DSP systems, and FPGAs. Each of these technologies has its own strengths and core capabilities in the areas of performance, development time, flexibility, and volume cost. Historically, most designs were based around only one or two of these processing technologies, but system designs now rely on multiple capabilities for differentiation and capability.

Systems that utilize the best features of each of these technologies are complex and difficult to integrate. Further, they require a significant investment in different tool flows (ASICs, DSP systems, FPGA systems, general-purpose processors) and personnel with varying design expertise that strains the design-productivity equation.

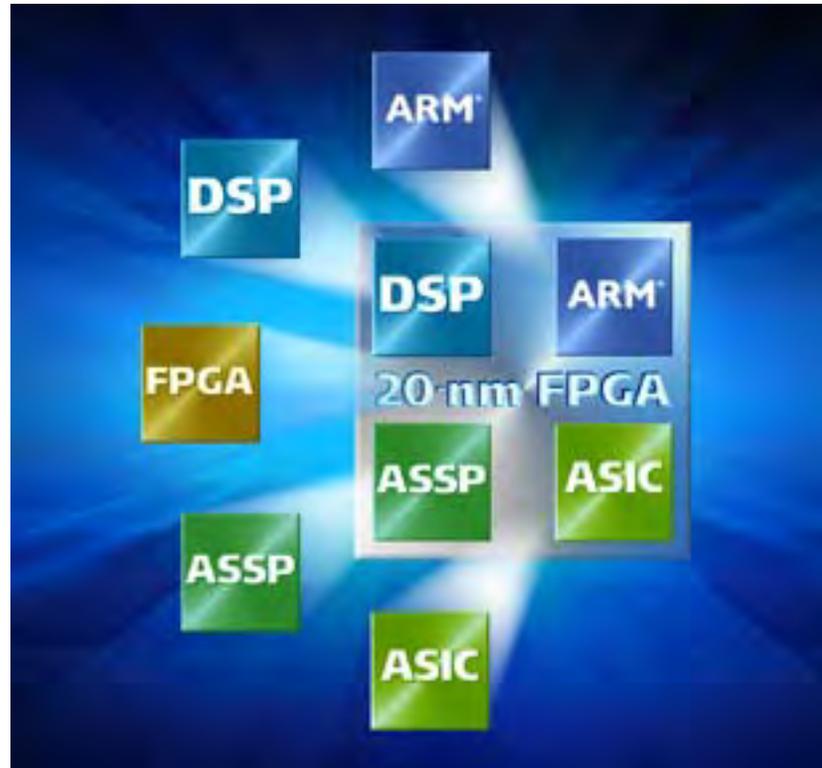
## 20 nm Process Technology Innovation

Advances in process technologies at 20 nm improve system capability in a variety of ways. The first is most commonly described by Moore's law as the steady reduction in silicon geometries. This leads to higher logic element, memory, transceiver, and other on-chip design resources. The second is an increase in performance and area efficiency through hardening standard IP such as memory controllers, communication protocols, general-purpose processing architectures, and DSP. This set of advancements is also made possible by the steady progress of Moore's law. A final driver of system capability is the integration of multiple silicon die into a single device using a standard silicon interface. These different drivers are often referred to by the International Technology Roadmap of Semiconductors (ITRS) and other industry groups as "More Moore" and "More than Moore" in reference to advances within the bounds and outside the bounds of Moore's law, respectively. <sup>(1)</sup>

## Multiple System Capabilities, One Fabric

A combination of the market forces and constraints mentioned above, as well as both planned and disruptive silicon technologies within and outside Moore's law, are now enabling classes of silicon devices and system-on-a-chip (SoC) solutions that integrate one or more of these technologies into a single monolithic or in some cases multichip solution (Figure 2). When examining each of these individual silicon-processing technologies, their overall technology roadmaps, and the economics of scale required to integrate multiple technologies, programmable logic companies are those best suited to provide for these converged silicon capabilities and tool flows. Altera's advantages in this area include design methodologies based on IP reuse, broad silicon product adoption across several markets, and highly leveraged partnerships with manufacturing partner TSMC and IP providers.

**Figure 2. Mixed-System Fabric Combines Different Silicon Capabilities into a Single Device**



Integrating multiple high-performance functions into a single silicon fabric requires either specialization in multiple processing technologies or the focus and effort to leverage an entire ecosystem of silicon IP and experience. Altera's primary partnership to enable the mixed-system fabric is with silicon manufacturer Taiwan Semiconductor Manufacturing Corporation (TSMC). By leveraging this twenty-year partnership through multiple manufacturing technology nodes, Altera is a primary user and driver of TSMC's Open Innovation Platform.<sup>(2)</sup> Through the sharing of corporate visions on silicon convergence, both Altera and TSMC can invest confidently in the manufacturability of converged silicon solutions.

Becoming a leading provider of 20 nm technology products requires a variety of other partnerships and integrated technology roadmaps. This drives Altera's partnerships with providers of electronic design automation (EDA) software for first access to 20-nm design software, manufacturers of DRAM and other memory providers, licensing of ARM® hard embedded processors, standards bodies for emerging memory technologies like Hybrid Memory Cube and design entry capabilities like OpenCL, and emerging optical internetworking bodies and forums.

## Enabling Silicon Convergence

Converging each of these technologies into one usable solution is enabled at 20 nm through a variety of software and hardware technologies. The first of these are system design tools like Qsys, as well as, OpenCL compilers, reference designs, and IP. Altera has been an industry leader in developing design tools innovations within Quartus® II software such as SOPC Builder and DSP Builder, enabled by a long-time vision of silicon convergence and commitment to enabling customers to take advantage of "More than Moore."

Also enabling silicon convergence is silicon-stacking technology using interposers and through silicon vias. This enables heterogeneous silicon systems that use different die fabrication technologies and optimizations, as well as highly differentiated mixed-system solutions. Some examples include direct low-latency connections to microprocessors, optical communication modules, dense memory blocks, and user-optimized HardCopy® custom ASICs. Altera is the only source for a mixed-system fabric that can enable very-high-density designs by combining a HardCopy ASIC and an FPGA. Bringing this capability to customers began with the announcement of chip-on-wafer-on-substrate (CoWoS) test chips with TSMC, and will culminate in 3D ICs available with 20 nm FPGAs.

3D stacked silicon devices will be available to Altera users through the use of a mixed-system digital interface designed to enable a broad variety of silicon and processing technologies to interface with the FPGA. Access to this interface is available to the Altera user community in order to promote 3D silicon innovations and provide an open forum to take advantage of “More than Moore” applications.

## **Next-Generation Transceiver Technology**

Altera’s next-generation 20 nm product families include a number of industry firsts such as monolithic 28 Gbps backplane-capable transceivers and 40 Gbps chip-to-chip transceivers, with a roadmap to achieve CEI-56G-compliant 56 Gbps transceivers for chip-to-chip and chip-to-module applications. Compared to the backplane-capable transceivers offered by Altera today, these latest innovations allow a 2X increase in bandwidth in wireline, military, and broadcast applications, and enable 8-lane 400 Gbps optical module communication.

Bringing unprecedented bandwidth to the backplane, the 28 Gbps backplane-capable transceivers have built-in pre-emphasis, equalization, dispersion compensation, and on-die instrumentation. These capabilities extend Altera’s well-established technology leadership to include emerging CEI-28G and 100GBase-KR4 backplane applications in areas such as wireline, OTN, high-capacity computing, and high-speed test systems.

Operating seamlessly with the other components of the mixed-system fabric, the transceivers in Altera’s 20 nm product families will play a key role in enabling industry roadmaps for next-generation products and protocols, while maintaining picjoule per bit energy-efficiency objectives.

## **Next-Generation Silicon Interconnect Technology**

Altera’s next-generation product families will introduce advanced 3D die-stacking technology to enable new classes of applications and a 10X increase in systems integration into a single device. This technology will feature a customer-accessible mixed-system digital interface standard enabling high-bandwidth, low-latency, and low-power solutions. The technology will enable FPGA integration with memory extensions (SRAM, DRAM), optical transceiver modules, user-optimized HardCopy ASICs, and third-party ASICs. This technology will enable the development of heterogeneous FPGAs that allow designers to mix and match IP based on end-user requirements. The applications of this 3D integration technology will be fueled by the innovations and creativity of the worldwide Altera user community.

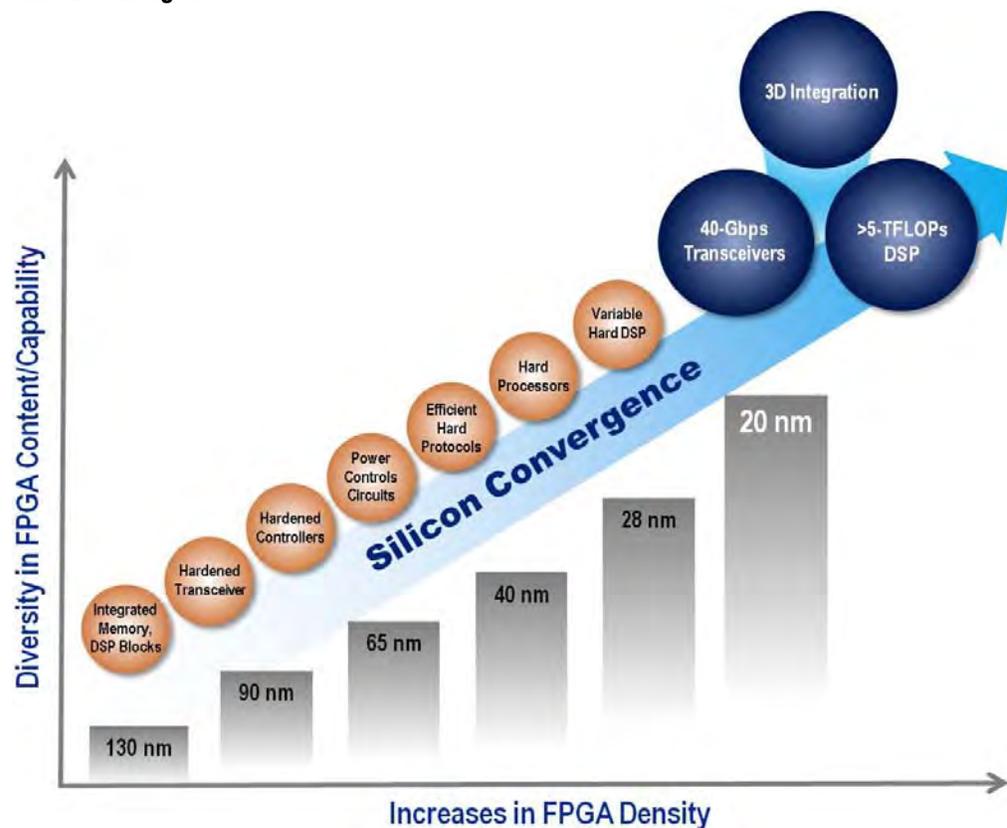
## Next-Generation High-Performance Design

DSP developers will no longer need to spend days and weeks trading productivity for performance in evaluating FPGA DSP solutions. Through the integration of OpenCL and Altera's next-generation variable-precision DSP block, Altera products will be able to achieve a 5X increase in floating-point processing performance while using a standard C-based design flow. With over 5 teraFLOPs of single-precision (IEEE 754) DSP performance, Altera will reset industry benchmarks in TFLOPs/watt efficiency. Applications of this very-high-performance DSP capability in a mixed-system fabric include high-performance and low-latency financial calculations, high-resolution broadcast and wireless, high-performance computing, and advanced military applications.

## Continuum of Silicon Convergence

FPGAs have been converging continuously over many process technology nodes. The innovations over time that lead to silicon convergence represent both the increase in logic density at these technology nodes, as well as hardened IP. These range from the first integration of on-chip memory, transceivers, memory controllers, and hardened protocols to power innovations, integrated soft and hard processors, enhanced system design tools, and the expanded capabilities enabled by the 3D digital silicon interface (Figure 3).

**Figure 3. Altera Has Steadily Increased the Diversity of FPGA Content, Continuing the Trend of Silicon Convergence**



## Conclusion

As convergence has driven more and more functionality and greater bandwidth into systems, Altera has responded with architectural innovations in mixed system fabric. From early innovations incorporating RAM, DSP multipliers, and transceivers, we have moved into a new architectural space—a space in which the distinction between hardened and programmable IP is determined by the customer’s need for differentiation; a space in which the edges of silicon dies and the boundaries of process technologies are no longer dividing lines between ICs. This also is a space in which high-level algorithmic descriptions become not just models, but actual designs. Today, we marshal these advances to help our customers produce systems that stand out in their markets: higher performance, more features, lower power, and the right cost. This is the measurable advantage Altera offers to its customers.

## Further Information

1. *More-than-Moore White Paper*, International Technology Roadmap for Semiconductors:  
[www.itrs.net](http://www.itrs.net)
2. TSMC Open Innovation Platform:  
[www.tsmc.com/english/dedicatedFoundry/services/oip.htm](http://www.tsmc.com/english/dedicatedFoundry/services/oip.htm)
3. System Technology at 20 nm and Beyond:  
[www.altera.com/20nm](http://www.altera.com/20nm)

## Acknowledgements

- J. Ryan Kenny, Product Marketing Manager, High-End FPGAs, Altera Corporation

## Document Revision History

Table 1 shows the revision history for this document.

**Table 1. Document Revision History**

Date	Version	Changes
September 2012	1.1	Minor text edits.
September 2012	1.0	Initial release.