
Challenges in Manufacturing Reliable Lead Free Components

Abstract

The recent push for lead free products is resulting in significant changes in packaging materials. Manufacturers of electronic equipment are requiring materials that consistently withstand peak reflow temperatures of 240° Celsius to 260° Celsius. Reflow soldering at these extreme temperatures, especially after extended moisture exposure, introduces several challenges that must be solved to produce reliable products.

Plastic packages use various organic compounds for molding and die attach that have formulations consisting of an epoxy resin, filler particles and other additives. The epoxy resin in equilibrium with the ambient atmosphere absorbs a small percentage of moisture, which turns into saturated steam during the printed circuit board reflow process. The extreme pressure from the steam and the drop in flexural strength of the mold compound and die attach materials can result in catastrophic failures of the packages. Typical failure modes of packages include encapsulant cracking, substrate cracking, severe package deformation, and delamination of one or more material interfaces. The problem is further exacerbated by the use of very large dies, which are typical of Altera® devices.

In this paper, we will discuss some of the modifications necessary to meet product reliability and usability requirements for lead free products. We will present the test results to demonstrate the reliability of plastic quad flat pack (PQFP), thin quad flat pack (TQFP), ball-grid array (BGA), and Flip-chip BGA components and relate the results to the different approaches that were taken for different package types to successfully qualify the components to the higher reflow temperatures. For some package families, the assembly processes were improved and optimized to ensure the reliability to Pb-free reflow temperatures. For some other components, new packaging materials were used to overcome the limitations of existing packaging materials.

We will also present effect of the reflow temperature on the moisture ratings of a representative member of each package family. In addition to the traditional responses such as pop-corning and interfacial delamination during reliability testing, the importance of looking at the effects of absorbed moisture on the component warpage at elevated temperatures will also be discussed. Absorbed moisture is known to increase package warpage. The higher warpage for large BGA components at Pb-free reflow temperatures requires the monitoring at the rated MSL, since it impacts the manufacturability and reliability of final assembly.

Introduction

Altera's Lead-Free (Pb-free) solutions are motivated by the requirements being imposed on the semiconductor and electronics industry to reduce or eliminate the use of Pb. A directive by European council on Waste from Electrical and Electronic equipment (WEEE) proposed restrictions on the use of Pb in electronics by 2006. In Japan, the ministry of international trade and industry has set a maximum amount of Pb for automobiles (excluding batteries). While there is no legislation mandating the reduction in Pb in the electronic devices in Japan, the electronic industry is actively marketing select electronic devices as Pb-free.

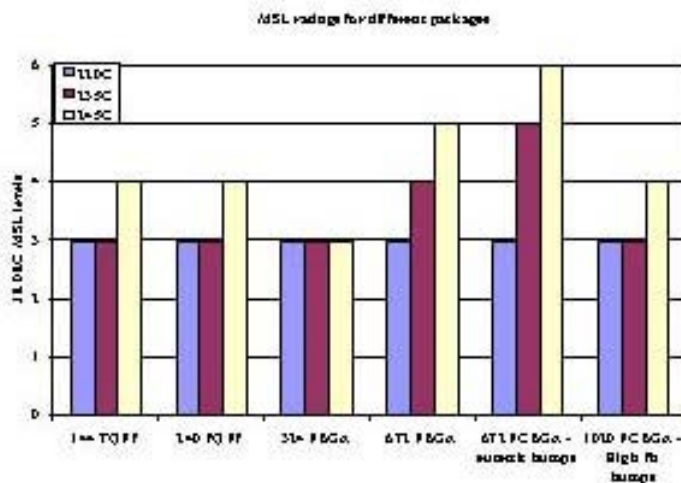
Based on these proposals and directives, Altera has proactively committed to working with its suppliers to offer Pb-free packaging solutions. There are several competing options available for Pb-free finishes. Working with the assembly sub-contractors Altera has evaluated packages with matte Sn and/or Sn-2% Cu lead finish for leaded packages, and Sn-3-4%Ag-0.5%Cu solder balls for ball grid array packages. Additional testing on pre-plated Ni/Pd finish is also being pursued as a possible alternative finish. For the leaded packages, 12 micron thick Sn or Sn-2% Cu plating is used on standard lead-frames. In addition to the change in the lead finish, the thermal robustness of the package was improved by selecting appropriate materials and processes to allow for the higher reflow temperature compatibility required for assembling boards using Pb-free solder pastes.

The qualification data gathered demonstrates the technical capability to assemble most devices offered by Altera with process and/or material modifications. Some of the devices tested had very large die sizes that posed some unique challenges. Not all available assembly process and materials strategies from the assembly sites were easily portable because of the very large die sizes for typical Altera devices. Various approaches were used to make the components reliable to Pb-free reflow temperatures, including the use of new materials and changes in the processes to achieve better reliability.

Verification of Moisture Sensitivity Levels

The standard Sn-Pb components without any additional modifications have been tested to the standard JEDEC surface mount simulation test to different Moisture Sensitivity Levels (MSL). The components were tested to different peak reflow temperatures – 220° Celsius, 235° Celsius, 245° Celsius. While almost all components meet MSL3 at 220° Celsius, some of the larger components meet only MSL4 or worse for higher temperatures (see Figure 1).

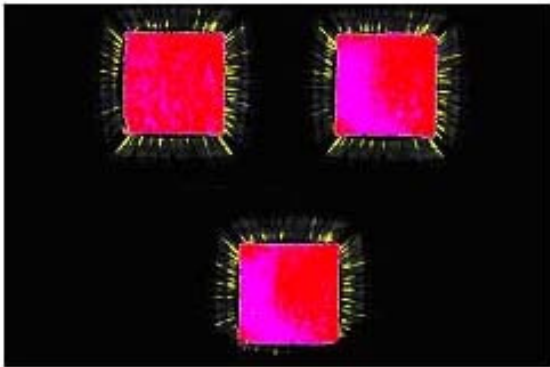
Figure 1. MSL Ratings for Standard Sn-Pb Components Tested to J-STD-020, for Different Peak Reflow Temperatures



For peak reflow temperatures of 245° Celsius testing on the larger components (and larger die sizes) resulted in die surface delamination (Figure 2) at MSL 3. Degradation in moisture sensitivity was

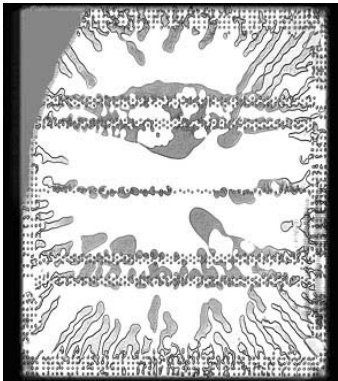
observed on each package type to different extents. Smaller TQFP, PQFP and FBGA packages were able to withstand 245° Celsius reflow.

Figure 2. Die Surface Delamination Observed on the Large QFP and FBGA Packages without Material/Process Modifications



For the case of Flip-Chip BGAs (FCBGA) underfill delamination and solder smearing (Figure 3) was observed when the solder bump composition was eutectic. When high Pb bumps were used, no underfill delamination was observed to 245° Celsius on all components 35mm on the side and smaller. Figure 3 shows underfill delamination and solder spreading/smearing was observed after preconditioning with a peak reflow of 245° Celsius when assembled with eutectic solder bumps.

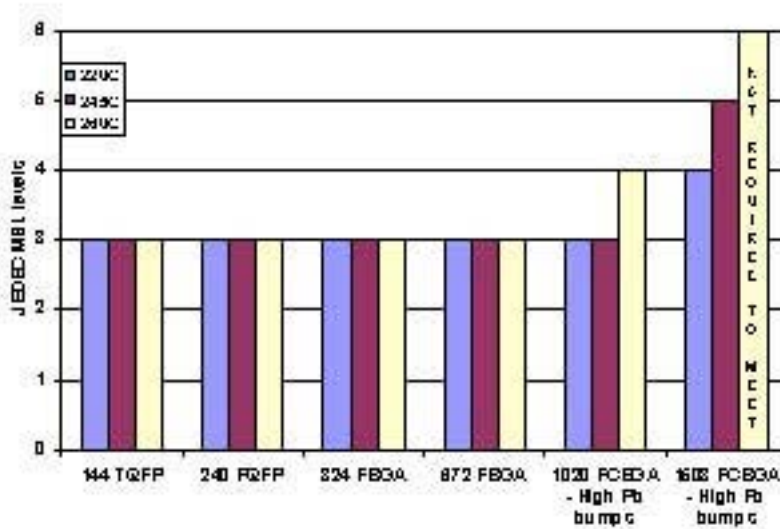
Figure 3. Underfill Delamination and Solder Spreading/Smearing Observation with a Preconditioning Peak Reflow of 245° Celsius when Assembled with Eutectic Solder Bumps



To improve manufacturability, Altera prefers to achieve MSL 3 rating for all the components. In order to achieve MSL 3 for all the components some modifications were necessary for each package type. Different approaches were required for each package type. Requirements from various industry groups require qualification of the components to a peak reflow temperatures of 245° Celsius to 260° Celsius depending on the component size.

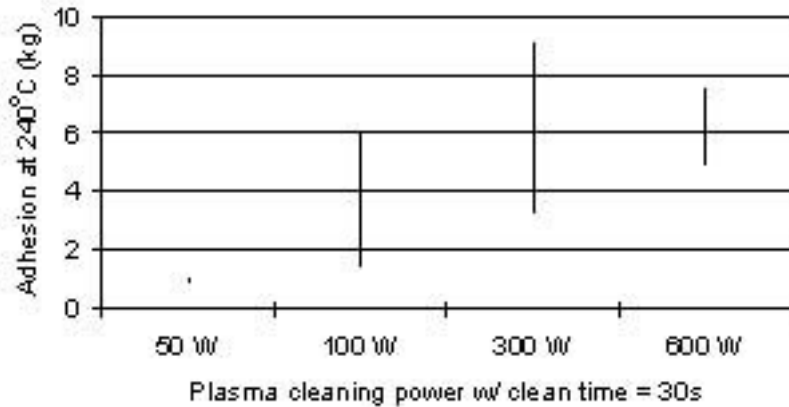
For the quad flat pack (QFP) packages, a new mold compound and a new die attach material had to be used to avoid package failures due to interfacial delamination and pop-corning. Part of the improvement comes from the lower moisture absorption rates for the new materials. Also, mechanical simulation models indicate that these materials result in a lower warpage for the components through the entire reflow temperature range, thereby resulting in lower stresses at all interfaces. Using the new material set JEDEC MSL rating of 3 can be achieved for all TQFP and PQFP packages, see Figure 4. In all cases, the standard lead frames were used. The Pb-free plating was either Matte Sn or Sn-2% Cu. Figure 4 also shows MSL ratings with the improvements to the material and assembly process flow. Most components meet MSL 3 to 260° Celsius peak reflow temperature.

Figure 4. MSL Ratings with the Improvements to the Materials and Assembly Process Flow



For the case of all Fine-line Ball Grid Array (FBGA) packages the mold compound and die attach used for the standard Sn/Pb assembly could be used with some minor variants. All devices tested in 19mm or smaller FBGA packages could meet JEDEC MSL 3 for reflow temperatures of 245° Celsius. However, for larger FBGA packages and for peak reflow temperatures above 245° Celsius die surface delamination was observed and additional modifications were required. All devices had a polyamide coating on the die surface. In the absence on the polyamide coating MSL rating of 3 would not be possible because of the very large die sizes. Two process changes were made to improve the adhesion of the mold compound to the die surface. Optimized pre-mold bake and die surface plasma cleaning steps were included to improve the adhesion of the mold compound to the die surface. It is believed that the surface roughening needs to be optimized to ensure good adhesion (Figure 5). With these improvements, JEDEC MSL rating of 3 was possible for all Altera devices in a FBGA package. There are some published reports in the literature indicating that AUS5 solder mask is not rated to the peak reflow temperatures required for Pb-free package. For that reason we have verified substrates with AUS5, AUS303 and AUS308 solder masks. In our testing, no failures related to the solder mask were observed for all tested combinations. Figure 5 shows data from sub-contractor showing the improvement in the mold compound adhesion to the roughened die surface (with polyimide coating) as a function of the plasma cleaning power for constant time.

Figure 5. Data from Sub-contractor Showing the Improvement in the Mold Compound Adhesion



Flip-chip BGAs (FC-BGA) are by far the most difficult packages to achieve JEDEC moisture level-3. Even if no failures were observed after preconditioning, often the components failed after 500 cycles of temperature cycling condition B stress. Typical failure mode was underfill delamination at the die corners (Figure 6). The use of 20mm and larger die sizes with 6000 or more solder bumps, adds additional complications. The selection of the correct choice of materials is important to achieve the MSL requirements while keeping the coplanarity of the components within manufacturable levels. In our initial testing it was obvious that eutectic Sn/Pb solder bumps could not be used for reflow temperatures exceeding 225° Celsius. The hydrostatic pressures in the underfill at the reflow temperatures cause the molten eutectic solder to smear along the surface of the die. This problem is so severe that the components can only survive the reflow in dry condition. For this and other reasons, Altera chose to use the high Pb bumps and eutectic pre-solder for all products. The overall composition of the bumps meets the European requirement of >85% Pb in the solder bump joints to be exempt for the time being. The softer nature of the high Pb bumps means that the tensile loading at the solder joints has to be minimized. Otherwise, the cyclic loading could result in pumping effects at the high Pb to Eutectic Sn/Pb interface causing voiding and solder joint opens. Figure 6 shows the die corner delamination seen on large die flip-chips with the old bill of materials. This failure mode was seen both for 220° Celsius and 245° Celsius reflow.

Figure 6. Die Corner Delamination Seen on Large Die Flip-chips with the Old Bill of Materials



In order to minimize the tensile and shear stresses at the solder joints a new set of materials was chosen for the underfill, thermal compound and the lid attach adhesive. Simulation models were used to identify most optimal material properties. The materials chosen for building the Pb-free (external only) flip-chips would allow us to rate most of the FC-BGAs to JEDEC moisture level 3. For the very large die (23mm on a side) and package sizes (40mm body) at this time even with the improvements only JEDEC level 5A can be achieved at 245° Celsius.

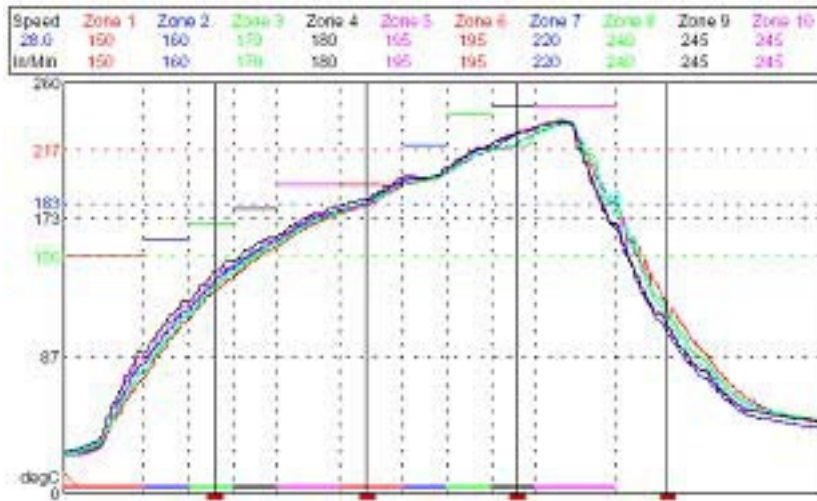
Is 260° Celcius Peak Reflow Temperature Required?

In addition to the standard component level testing, on component for each package type was mounted on to PC boards to verify the solder joint reliability. The devices were mounted onto PC boards at Solecron Corporation using ten zone production reflow oven. The oven was purged with Nitrogen during the reflow process. The reflow profile was optimized for each device separately. Kester 256-LF, an Alkaline no-clean flux, was used for mounting all three devices. Components were mounted both with and without Nitrogen ambience to estimate the lowest temperature at which the components can be mounted. A representative reflow profile is shown in Figure 7. The reflow profile shown in Figure 7 is used for surface mount of 780 pin FC-BGA package.

- Peak reflow temperature was 236° Celsius.
- The devices were mounted in air.
- Time above melting point was 70s.

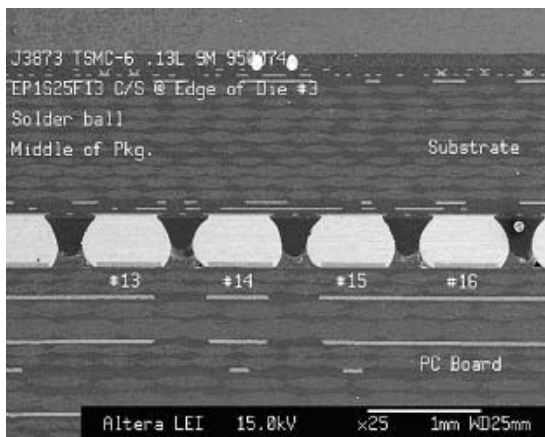
Cross-section showing the solder joints is also shown in Figure 7. In addition to the standard board assembly rework assembly was also studied for the Pb-free components. Detailed results of this work will be presented at APEX-2004 meeting in San Diego [1]. The peak temperature required for board assembly of large components can be as low as 235° Celsius even when mounted in air.

Figure 7. Reflow Profile used for Surface Mount of 780 pin FC-BGA Package



A cross-section view of the solder joints is shown in Figure 8. From the cross-section it is clear that large components can be mounted at temperatures as low as 235° Celsius. Even assuming a variation of about 15° Celsius across a large board, it is feasible to mount a wide range of components at peak temperatures not exceeding 250° Celsius at any point on the board. In our opinion, requiring all components to be reflowed at 260° Celsius is putting an enormous and unnecessary burden on the component suppliers. Figure 8 shows the cross-section of a 780 pin FCBGA Device, showing good collapse of the Pb-free solder joints for a peak reflow temperature of 235° Celsius.

Figure 8. Cross-section of a 780 pin FCBGA Device Showing Pb-free Solder Joints



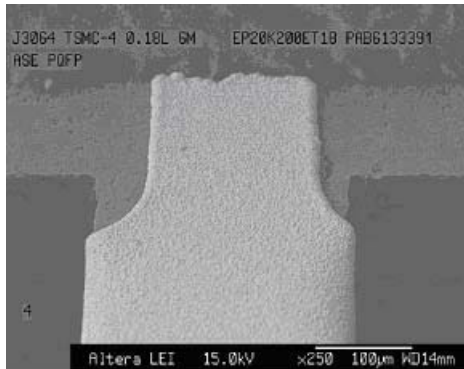
Whisker Growth on Leaded Packages

There have been several reports published on pure tin finishes being susceptible to the spontaneous growth of single crystal structures known as “Tin Whiskers”. Tin whiskers can cause electrical failures, ranging from Parametric deviations to catastrophic short circuits. Although the tin whisker phenomenon has been reported and studied for decades, it is still a potential reliability hazard, particularly where the equipment is subject to long term storage before use. There have been several attempts to devise a reliable test to accelerate the growth of these whiskers, but so far all results appear to be applicable for a specific plating process. In the absence of a test method for acceleration of the Tin whisker growth, we chose to look at components stored at room temperature for extended periods of time to verify the Tin whisker growth phenomenon. Some five units were visualled after assembly, 30 days storage, 180 days storage and 450 days storage. In addition to inspection of components stored at ambient conditions, inspection was performed on five components after completion of the reliability tests (preconditioning, Biased Humidity test and Autoclave). In all cases, 20 leads were visualled at 20X, 100X and 250X magnification. A sample image is shown in Figures 9 and 10 for Matte Sn and Sn-2%Cu finish leads, respectively. The images were for devices that have been stored at room temperature for 450 days. The plating thickness was 12 microns for both finishes. No whisker growth was observed in all cases. From our observations, it appears like by controlling the plating process, the lead-frame material and the plating thickness, it is possible to avoid Tin whiskers. Figure 9 shows a sample aged for 450 days. The coarse grains give the finish a matted appearance. No whiskers were observed.

Figure 9. High Magnification View of a Matte Sn Finished Lead on a PQFP Device



Figure 10. High Magnification View of a Matte Sn-2%Cu Finished Lead on a PQFP Device Aged for 450 Days



Component Warpage at Pb-free Reflow Conditions

Component warpage plays a critical role in the manufacturability of very large BGA components. A paper presented by Shook et al. [2], showed that the ingressed moisture increases the warpage even further when tested with ingressed moisture. In our case, all the large BGAs use Flip-Chip interconnections. We studied the warpage behavior of large flip-chip devices with and without subjecting the packages to moisture loading. The FC-BGAs typically have the highest warpage at room temperature and tend to flatten out at reflow temperatures. There was approximately 10% difference observed in the measured warpage at room temperature between the dry and moisture soaked devices. At reflow temperatures the warpage continued to be higher for the device soaked in moisture. Subsequent C-SAM analysis showed no delamination in the package. Also, components have reduced warpage upon bake and are indistinguishable from the dry components. Our observations are consistent with the observations made by Shook et al. However, in no case the warpage was above our internal specification of 8mils. Warpage measurements at room temperature and peak reflow temperature are shown in Figures 11 and 12 for dry and moisture soaked devices. The measurements were done on a 33mm package. Similar results were observed on a 27mm wire-bonded FBGA package.

Figure 11 shows the warpage measurements on a 33mm package after 192h of moisture soak at 30° Celsius and 60% RH. The peak warpage of 5.6mils was observed at room temperature (top). At reflow conditions the warpage was stable at ~2mils (bottom). No delamination was observed.

Figure 11. Warpage Measurements on a 33mm Package after 192h of Moisture Soak at 30° Celsius and 60% RH

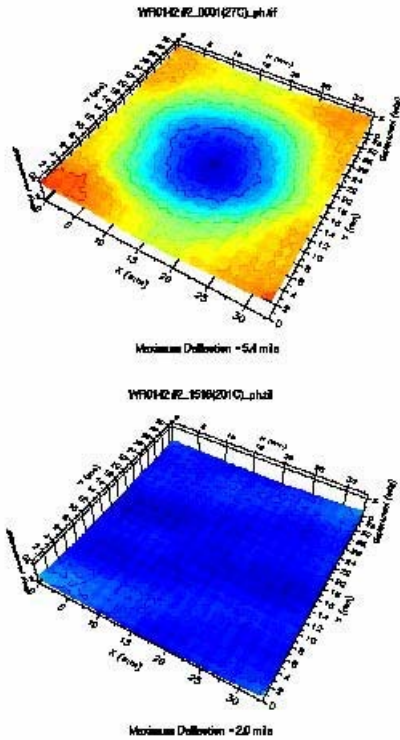
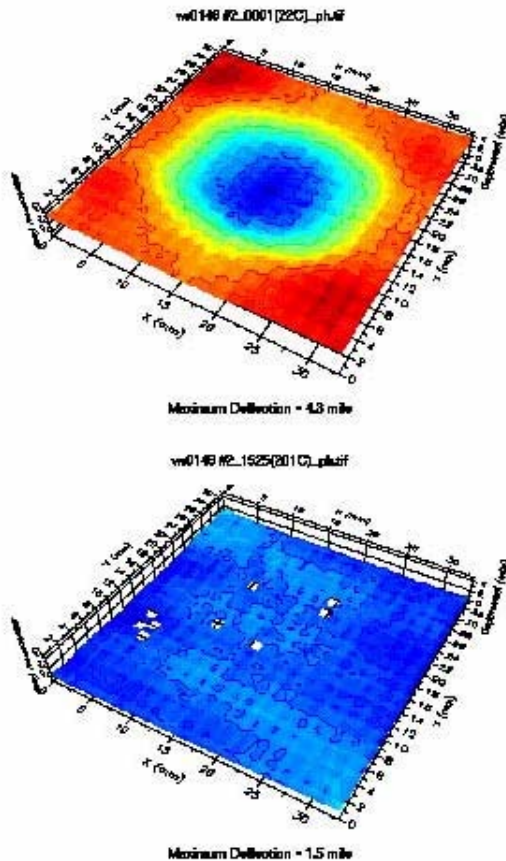


Figure 12 shows the warpage measurement on a 33mm package in the dry condition. The peak warpage of 4.3 mils was observed at room temperature (top), At reflow conditions the warpage was stable at ~1,5 mils (bottom).

Figure 12. Warpage Measurements on a 33 mm Package in the Dry Condition



Conclusions

Several years of Pb-free research has concluded that there is no drop-in solution to replace Pb-Sn solder in electronics industry. However, the industry has accepted the use of eutectic Sn-Ag-Cu for solder balls and either Matte Sn or Sn-2%Cu for lead finishes. We tested components with these finishes to confirm that most components can be manufactured and assembled onto boards reliably. We have shown that with suitable modifications of the component assembly processes and materials, it is possible to manufacture reliable TQFP, PQFP, FBGA and FC-BGA package families. Further, we have shown that the requirement of 260° Celsius reflow temperature is excessive and boards can be assembled and reworked without exceeding a peak reflow temperature of 250° Celsius. Also, work done on warpage on large flip-chip BGAs shows that moisture ingress could play a role in determining the moisture rating of the components.

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Finally, authors would also like to thank Jasbir Bath and Samson Lam of Solectron and Sam Yoon for help in board assembly and discussions on second level reliability of the Pb-free components.

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1. *Board Assembly and Rework of Large Flip-Chip Ball Grid Array Devices*, Sam Yoon et al, Apex-2004 to be published
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