
Stratix II vs. Virtex-4 Power Comparison & Estimation Accuracy

Introduction

This document compares power consumption and power estimation accuracy for Altera® Stratix® II FPGAs and Xilinx Virtex-4 FPGAs. The comparison addresses all components of power: core dynamic power, core static power, and I/O power. This document uses bench-measured results to compare actual dynamic power consumption. To compare power estimation accuracy, the analysis uses the vendor-recommended power estimation software tools. The summary of these comparisons are:

- Altera's Quartus® II PowerPlay power analyzer tool is accurate (to within 20%), while Xilinx's tools are significantly less accurate.
- Stratix II devices exhibit lower dynamic power than Virtex-4 devices, resulting in total device power that is equal.

Having an accurate FPGA power estimate is important to avoid surprises late in the design and prototyping phase. Inaccurate estimates can be costly and cause design issues, including: board re-layout, changes to power-management circuitry, changes cooling solution, unreliable FPGA operation, undue heating of other components, and changes to the FPGA design. Furthermore, without accurate power estimates, it is impossible for the designer and FPGA CAD software to optimize design power.

This white paper contains the following sections:

- Components of total device power
- Power estimation and measurement methodology
- Core dynamic power comparison – power tool accuracy and bench measurements
- Core Static power comparison
- I/O power comparison
- Total device power summary

For competitive comparisons on performance and density between Stratix II and Virtex-4 devices, refer to the following white papers from the Altera web site:

- *Stratix II vs. Virtex-4 FPGA Performance Comparison White Paper*
- *Stratix II vs. Virtex-4 Density Comparison White Paper*

Components of Total Device Power

Total device power is the sum of three components: core dynamic power, core static power, and I/O power. Core dynamic power is the power dissipated by the operation of the FPGA core fabric. This power increases linearly with operating frequency. Core static power is the power dissipated that is independent of frequency (such as leakage current across a transistor) and can be determined by stopping all clocks (an operating frequency of 0 MHz). The final power component, I/O power, is the power dissipated in the FPGA I/O cells to communicate with other chips. Figure 1 shows the breakdown of power into these three components for the average Stratix II design. This data was obtained by estimating the power consumption of 99 complete designs with the Quartus II software version 5.0 SP1 PowerPlay power analyzer.

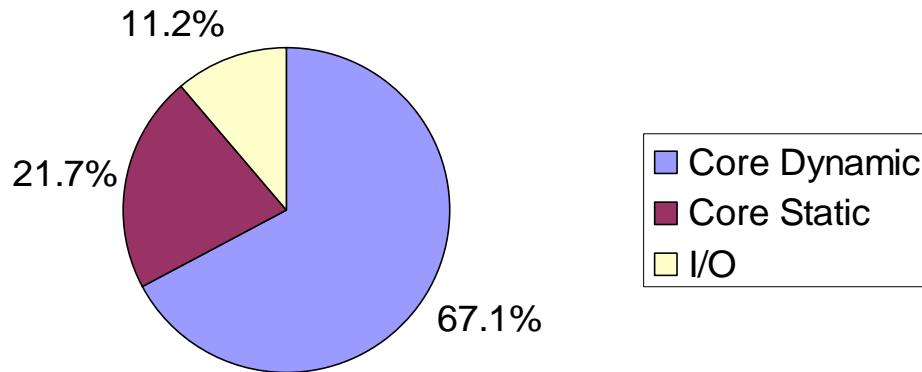


Figure 1. Average Breakdown of Total Power in Stratix II Designs (Typical Conditions, 12.5% Toggle Rate)

The data in Figure 1 uses the 3.3-V LVTL I/O standard with 10-pF output loading. In addition, Figure 1 reflects static power at typical conditions. At worst-case conditions, the proportion of static power will increase. Figure 1 shows that static power is on average 21.7% of total device power which is relatively significant compared to previous generation FPGAs. However, core dynamic power remains the most important portion of total device power.

Power Estimation & Measurement Methodology

FPGA vendors provide power estimation tools to help users design the board power supply and the system cooling solution. These power estimation tools also help designers optimize device power consumption. Altera tools generate power estimates based on parameters such as design resource utilization, routing utilization, clock frequencies, device, I/O loading, temperature, and silicon process. Each of these parameters can affect static power, dynamic power, or both.

Stratix II static power is primarily affected by device junction temperature, voltage, and silicon process variation. Altera supplies typical and worst-case power specifications. These specifications are based on silicon characterization performed across a wide array of devices across various extremes of silicon process variation. All devices shipped meet the worst-case specification, and this specification should be used in the design of system thermal solutions.

Dynamic power is primarily affected by design resource utilization, design implementation, routing utilization, and circuit switching activity. Silicon process and temperature variation have very little effect on dynamic power. A power model of each element within the Stratix II FPGA enables accurate power estimation. If a designer knows the design information (such as utilization, frequency, or I/O loading), then an estimation of power can be made. Either the designer can make an educated guess of the design information or compile the design to gain more accurate design information.

Altera's Power Estimation Tools

There are three primary methods of assessing the power consumption of a Stratix II design, which are listed as follows, from least accurate to most accurate:

Stratix II PowerPlay Early Power Estimator Spreadsheet. This spreadsheet generates design power estimates based on user-entered resource utilization, toggle rates, and environmental conditions. The early power estimator is used prior to design implementation and as a result, accuracy of the power estimation data is dependant on the accuracy of the design information entered by the user. The power model used in this tool is based on the model in the Quartus II PowerPlay power analyzer tool, but assumes typical logic implementation and routing utilization. The analogous Xilinx tool is the Web Power Tool (WPT). The early power estimator accuracy is generally within $\pm 20\%$ of the Quartus II PowerPlay power analyzer estimates, assuming perfect toggle-rate entry.

Quartus II PowerPlay Power Analyzer. The PowerPlay power analyzer is integrated in the Quartus II software and generates design power estimates based on Quartus II software place-and-route information and toggle rate data from a variety of sources. The power analyzer performs power analysis based on the exact resources, logic functions, and routing paths used in the target design. It can derive toggle rates from user entry, statistical circuit analysis techniques, RTL simulation, and gate-level simulation. The power analyzer can optionally filter out pulses, or glitches, from simulation data when those glitches are too fast to toggle the logic and routing of an actual FPGA. The highest-quality estimates are found when using the Power Analyzer with glitch-filtered gate-level simulations.

Unless noted, this document shows results comparing Quartus II software version 5.0 SP1 PowerPlay power analyzer estimations to Stratix II bench results, demonstrating estimation error within $\pm 20\%$, with a bias toward over estimation. Results for the analogous Xilinx tool, ISE XPower 7.1 SP2, are shown alongside Virtex-4 bench results, with estimation error results that range from a $8\times$ underestimation to $3\times$ overestimation.

Bench Measurements. The best estimate of a design's dynamic power is obtained by measuring a design in-system. This is done by measuring the amount of current the FPGA is drawing on each power rail at the required frequency.

Static power results from single-unit measurements are not meaningful due to significant unit-to-unit static power variation. The vendor-provided worst-case specification should be used instead (as explained in the static power consumption section of this document).

Use the following steps to obtain a worst-case estimate for total device power in-system:

1. Measure the power drawn from each power supply voltage from a device configured with the correct I/O standards and phase-locked loop (PLL)/digital clock manager (DCM) usage, with a 0-MHz clock. This provides the baseline static power consumption for the FPGA.

$$P_{unconfigured_static,measured} = \sum_{i \in \text{All supplies}} I_i \cdot V_i \quad (1)$$

2. Program the FPGA with the design-under-test and measure the power drawn from all power rails with each clock running at its target frequency. This provides a measurement of total power (dynamic and static power).
3. Compute the worst-case total power of a device running this design by adding in the difference between the static power of this device measured in #1 and the vendor-supplied worst-case

specification for static power (using the correct I/O standards and phase-locked loop (PLL)/digital clock manager (DCM) usage).

$$P_{Total, worst-case} = P_{Operation, measured} + (P_{static, worst-case-spec} - P_{unconfigured_static, measured}) \quad (2)$$

Altera designed and developed a power test board to compare Stratix II and Virtex-4 power consumption. This board, shown in Figure 2, has two electrically isolated halves, one with a Stratix II EP2S60 device and the other with a Virtex-4 LX60 device. The two board halves are identically designed except where device requirements require small differences. The FPGA power rails are isolated and individually regulated, allowing for precise measurements of supply current per power rail. I/O traces for each device are matched in length to allow for accurate I/O power comparisons.

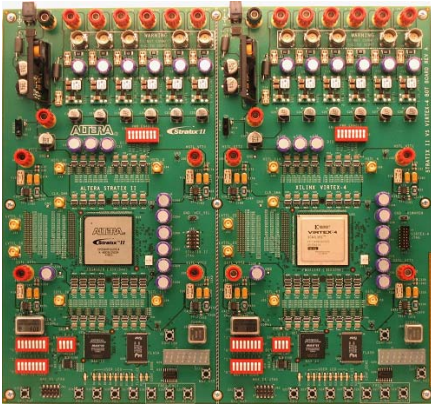


Figure 2. EP2S60 & LX60 Board Used for Comparing Dynamic & I/O Power

For more information on Altera's power estimation tools, see the Power Estimation & Analysis section in the *Quartus II Development Software Handbook*.

Dynamic Power Comparison: Stratix II vs. Virtex-4 FPGAs

To compare the dynamic power of a Stratix II device to a Virtex-4 device, Altera compared measured and estimated results across a variety of designs selected to provide coverage of many types of FPGA functions.

Circuits were coded in an architecture-independent hardware description language (HDL) wherever possible. In some cases, such as RAM designs, the respective MegaWizard® Plug-In Manager or Core Generator tools were used to generate designs with matching parameters. Stratix II designs were compiled using the Quartus II software version 5.0 SP1, using the Standard Fit option and a tight timing constraint. Virtex-4 designs were compiled using Synplify Pro 8.1 for synthesis and ISE 7.1 SP2 for place-and-route. Each design was constrained to the achievable f_{MAX} in order to ensure maximum place-and-route effort.

Each design was measured on both devices using the power test board described above. The designs include random vector generators that were used to reduce external stimulus requirements to just a clock and enable signal as inputs. Power was measured by sweeping the input clock frequency from 0 MHz to the maximum allowable operation frequency (f_{MAX}). To isolated dynamic power, the power measured at 0

MHz (static power) was subtracted from each power measurement at each frequency point. Since dynamic power increases linearly with frequency, the best-fit line of all the dynamic power points is taken as dynamic power, represented as mW/MHz in this document. For each design the mW/MHz value for both Stratix II and Virtex-4 devices are compared using the formula:

$$\% \text{ Dynamic Power Difference} = \frac{(\text{Stratix II Dynamic Power} - \text{Virtex-4 Dynamic Power})}{\text{Virtex-4 Dynamic Power}}$$

The power was also estimated using the Quartus II software version 5.0 SP1 PowerPlay power analyzer and the ISE 7.1 SP2 XPower software. Toggle rates were derived by supplying each tool with a Value Change Dump (VCD) file produced from a ModelSim gate-level timing simulation. The applied vectors are identical what was used in bench measurements.

The bench measurements were compared to the power estimates from the tools using the formula:

$$\% \text{ Estimation Error} = \frac{(\text{Estimated Dynamic Power} - \text{Measured Dynamic Power})}{\text{Measured Dynamic Power}}$$

Executive Summary of Dynamic Power & Power Estimation Accuracy Results

Figure 3 compares the bench measurements with the estimates of Quartus II software version 5.0 SP1 PowerPlay power analyzer and ISE 7.1 SP2 XPower. The 20 designs were selected to provide coverage of many typical FPGA functions. The PowerPlay power analyzer results are within 20% of silicon, while XPower results show a significant spread, underestimating by up to 8× and overestimating by up to 3×.

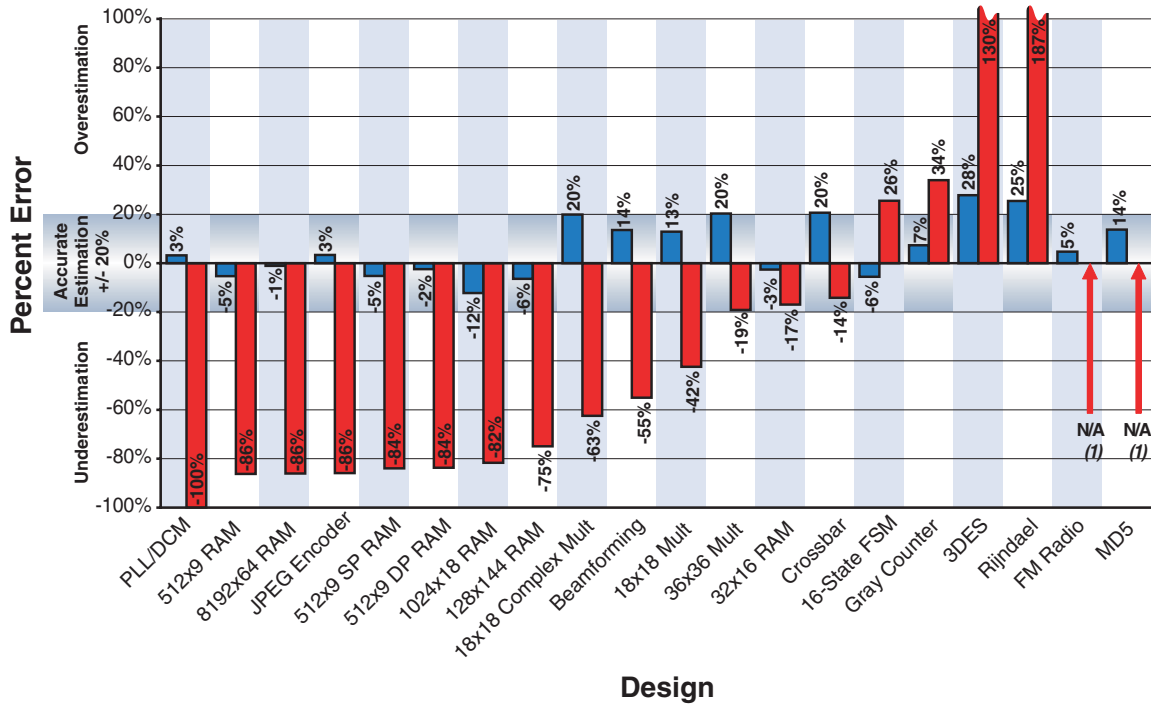


Figure 3. Estimation Error of Dynamic Power for 20 Individual Designs from Quartus II PowerPlay & ISE XPower

Note to Figure 3:

(1) The Xilinx ISE XPower tool crashes when reading large or complex Value Change Dump (.vcd) files. No XPower estimates are available for these designs

Figure 4 shows the dynamic power measurements for Stratix II devices relative to Virtex-4 devices (Stratix II dynamic power divided by Virtex-4 dynamic power). The same 20 designs were used from Figure 3, which include test designs that focused on specific blocks of the devices and real-world designs with more broad utilization. Stratix II devices exhibit a substantial power advantage on nearly all RAM configurations, and consume equivalent or better dynamic power in block-level logic and DSP designs. Even in a 1,024 × 18 RAM application that optimally maps to Virtex-4 device BRAM, Stratix II devices are only at a 21% disadvantage compared to the 5× factor claimed by the competition. On complete, user designs including an MD5 cryptographic hash function, an FM Radio transceiver, a 3DES cipher core, a Rijndael core, and a JPEG encoding core, Stratix II devices exhibit up to 54% lower dynamic power. The Beamforming design is a full HDL customer RADAR imaging application that employs DSP blocks, RAM blocks, and logic. The Beamforming result shows that Stratix II FPGAs have a 47% advantage.

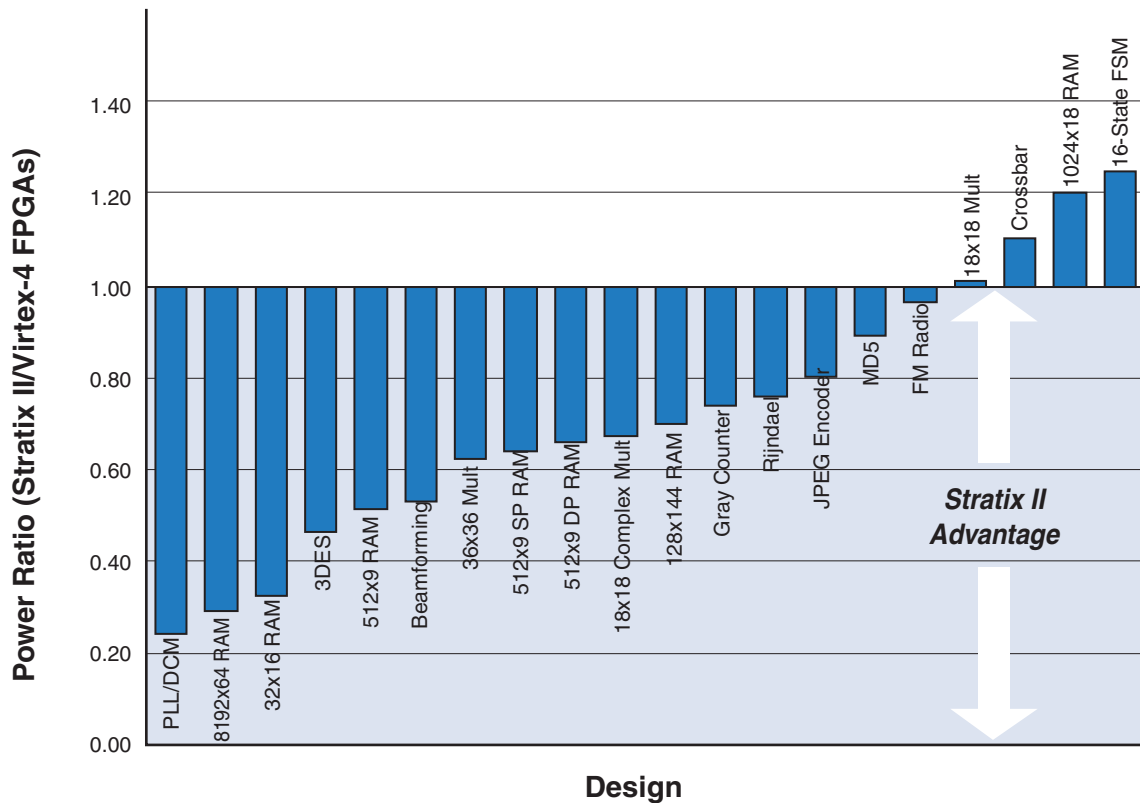


Figure 4. Dynamic Power Ratio (Stratix II vs. Virtex-4), Based on Hardware Measurements

User Logic & Routing Power

Table 1 provides bench results for a set of Stratix II and Virtex-4 logic design tests. The designs include:

- 16-State FSM – a 16-state Finite State Machine.
- Gray Counter – a counter for the Gray code binary numeral system.
- 32-bit 32×8 Crossbar – 32-bit wide, 32 channel to 8-channel cross-bar switch.
- FM Radio – an LE-based FM receiver that does not make use of the hard digital signal processing (DSP) functions available in either device.
- MD5 – a cryptographic hash function.
- Rijndael – an implementation of the AES encryption algorithm.

Table 1: Bench-Based Logic Function Power Comparison with Estimation Error

Design	Hardware Measured Dynamic Power (mW/MHz)			Estimation Error (“+” is Overestimate, “-” is Underestimate)	
	Stratix II EP2S60	Virtex-4 LX60	Stratix II to Virtex-4 Power Difference (%)	Quartus II PowerPlay Analyzer	ISE XPower
16-State FSM	11.31	9.05	+25%	-5%	+26%
Gray Counter	12.49	16.90	-26%	+7%	+34%
Crossbar	19.74	17.85	+11%	+20%	-14%
3DES	48.44	104.52	-54%	+28%	+130%
FM Radio	63.23	65.53	-3%	+5%	N/A (1)
MD5	41.83	46.82	-11%	+14%	N/A (1)
Rijndael	12.78	16.80	-24%	+25%	+187%

Note to Table 1:

(1) The Xilinx ISE XPower tool crashes when reading large complex Value Change Dump (.vcd) files. No XPower estimates are available for these designs.

In general the Quartus II software estimates power within 20% of the measured value, and has a safe over-estimation bias. ISE XPower results show an estimation error significant spread, underestimating by 14 percent (Crossbar) and overestimating by almost 3× (Rijndael).

The Quartus II PowerPlay power analyzer overestimated two designs by 25% and 28%. These designs are by nature designs that will be overestimated. The cause for the overestimation lies at the gate level simulation of the design. The simulator and Quartus II PowerPlay power analyzer work together to ensure the resulting simulation waveforms do not contain spurious transitions. Some glitching events are too short to actually propagate in a real chip and thus should be ignored for good-quality power estimates. Since the glitch filtering technology is designed to be conservative, it is possible that some spurious transitions are left in the simulation waveforms, while they do not actually occur in silicon. The ISE XPower overestimates power by 187% and 130% for these same designs.

When comparing dynamic power consumed, the larger user designs including an MD5 cryptographic hash function, an FM Radio transceiver, a 3DES cipher core and a Rijndael encryption core, Stratix II devices exhibit up to 54 percent lower dynamic power.

Memory Power

Both Stratix II and Virtex-4 FPGAs contain embedded memory in their core fabric. Stratix II devices incorporate three sizes of RAM blocks: 512 bit, 4.5 Kb, and 576 Kb. Virtex-4 devices incorporate two sizes of RAM blocks: 16 bit and 18 Kb.

FPGA RAM block power is affected by the size (width and depth) and the actual implementation of the RAM block in the FPGA. Figure 5 shows two ways that the Quartus II software can implement a 1,024 × 16 RAM block out of four M4K RAM blocks. The area-optimized method (on the left) splits the logical RAM word across four memory blocks and accesses each RAM block every cycle. This results in an estimated 27 mW of power. The power-optimized method (on the right) uses a decoder, multiplexer, and four RAM blocks, each of the same width as the logical RAM word; this hardware is automatically generated by the Quartus II RAM megafunction. The result is only one of four M4K blocks is active on any cycle, reducing overall power from 27 mW to an estimated 12.9 mW. This estimate includes the additional power consumed by the decode and multiplexer logic.

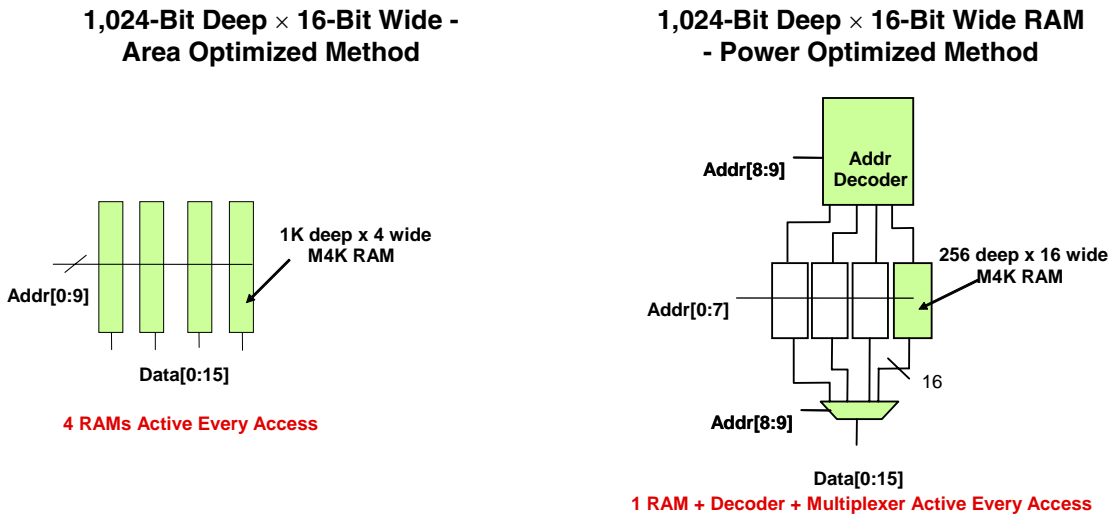


Figure 5. Area- vs. Power-Optimized Implementations of a 1,024-Bit Deep × 16-Bit Wide RAM

Altera compared Stratix II and Virtex-4 RAM power on the bench for a variety of RAM sizes. For each design, many copies of the desired RAM block were instantiated to use as many RAM blocks as possible without saturating the capacity provided by either device. The RAM address and data inputs and read/write enables were driven by pseudo-random data streams generated via on-chip linear-feedback shift registers. The power shown in Table 2 includes the power consumed in the test logic, routing, and RAM blocks. Unless otherwise noted, the designs use registered simple dual-port (one read, one write) RAMs.

Table 2: Bench-Based RAM Function Power Comparison with Estimation Error

Design (Depth × Width)	Hardware Measured Dynamic Power (mW/MHz)			Estimation Error ("+" is Overestimate, "-“ is Underestimate)	
	Stratix II EP2S60	Virtex-4 LX60	Stratix II to Virtex-4 Power Difference (%)	Quartus II PowerPlay Analyzer	ISE XPower
32 × 16	2.42	7.42	-67%	-3%	-17%
512 × 9	2.25	4.37	-49%	-5%	-86%
128 × 144	4.02	5.74	-30%	-6%	-75%
1,024 × 18	2.11	1.75	+21%	-12%	-82%
8,192 × 64	0.67	2.30	-71%	-1%	-86%
512 × 9 (single port)	2.08	3.25	-36%	-5%	-84%
512 × 9 (true dual port)	4.06	6.14	-34%	-2%	-84%

The Stratix II device uses less power by a wide margin on most of the designs. The 32 × 16 design compares Virtex-4 distributed RAM to Stratix II M512 RAM blocks. The Stratix II dedicated RAM blocks consume significantly less power than the distributed solution used in the Virtex-4 device. Similarly, the Stratix II device has an advantage on the 512 × 9 and 8,192 × 64 RAM blocks because they map efficiently to the M4K and M-RAM blocks, respectively. Despite the 18K size of the Virtex-4 BRAM, the Stratix II device consumes less power when implementing one of the 18K RAM block designs (128 × 144) while

consuming only 21% more power on the other ($1,024 \times 18$) compared to the Virtex-4 device's optimal RAM configuration.

These results also show that the Quartus II PowerPlay power analyzer consistently estimates the overall power for these designs to within 20% of device measurements. XPower, on the other hand, consistently underestimates power for the BRAM, and does so by a wide margin. In the case of the $8,192 \times 64$ design, XPower underestimates dynamic power by a factor of 8.

The Stratix II TriMatrix™ memory architecture provides the correct memory size more often and, as a result, provides the lower overall memory power solution.

DSP/Multiplier Power

Stratix II and Virtex-4 FPGAs both contain embedded DSP blocks in their core fabric. The Stratix II DSP block offers multipliers, adders, subtractors, accumulators and a summation unit—functions that are frequently required in typical DSP algorithms. Each DSP block can support a variety of multiplier bit sizes (9×9 , 18×18 , 36×36) and operation modes (multiplication, complex multiplication, multiply-accumulation and multiply-addition). The Virtex-4 DSP48 block also offers multipliers, adders, subtractors, accumulators and a summation unit, but are lacking in some implementation efficiencies that impact power. One example of this is that four Stratix II 18×18 multipliers can aggregate into a single 36×36 multiplier, while the Virtex-4 DSP48 slice cannot aggregate to a single cycle 36×36 multiplier.

Similar to the RAM test designs, Altera instantiated Stratix II DSP and Virtex-4 DSP48 blocks using Quartus II megafunctions and ISE CoreGen tools, and stimulated them with pseudo-random data streams. In addition to simple multiplication, these tests include a complex 18×18 multiply ($A \times B + C \times D$). The results from these tests are shown in Table 3.

Table 3: Bench-Based DSP Function Power Comparison with Estimation Error

Design (Depth \times Width)	Hardware Measured Dynamic Power (mW/MHz)			Estimation Error ("+ is Overestimate, - is Underestimate)	
	Stratix II EP2S60	Virtex-4 LX60	Stratix II to Virtex-4 Power Difference (%)	Quartus II PowerPlay Analyzer	ISE XPower
18×18 multiplier	3.45	3.40	+1%	+12%	-42%
36×36 multiplier	3.11	5.00	-37%	+20%	-19%
18×18 complex multiplier	4.97	7.36	-32%	+19%	-62%

Both Stratix II and Virtex-4 DSP architectures are designed to efficiently support 18×18 multiplication in silicon, as the power consumed in both shows a 1% difference. The Stratix II DSP architecture shows a larger advantage on 36×36 multipliers and complex multiplications, which take advantage of dedicated hardware. Virtex-4 devices use four 18×18 multipliers plus a 27-bit external adder to emulate a 36×36 multiplier. This extra logic and the programmable routing results in 37% lower power for the Stratix II hard-multiplier solution.

The estimation tool results show that the Quartus II PowerPlay power analyzer consistently estimates the overall power for these designs to within 20% of silicon measurements. XPower, on the other hand,

consistently underestimates power for these designs, and does so by a wide margin. XPower underestimates dynamic power by 62% for the 18×18 complex multiplier design.

PLL & DLL Power

Stratix II employs analog PLLs for clock synthesis and shifting, while Virtex-4 uses Digital Clock Managers (DCMs) or digital DLLs. To compare the power of these blocks, Altera created a design using four PLLs or DCMs configured to generate a 300-MHz clock, and measured the power drawn on the bench. It is important to consider both static and dynamic power contributions since PLL/DCM circuits can draw power even when no clock is applied. Also, the DCM draws considerable power from 2.5-V V_{CCAUX} power rail on the Virtex-4 device, so it is important to measure both core power supplies (V_{CCINT} and $V_{CCPD/AUX}$).

Figure 6 graphs the bench-measured power for a design containing four PLLs or DCMs. The y-intercept of the Virtex-4 data is non-zero and indicates a high static power component (112 mW or 28 mW per DCM) as compared to the negligible static power of the Stratix II PLL (3 mW per PLL). The dynamic power of the Virtex-4 DCMs is nearly 4× that of the Stratix II PLLs, indicated by the higher slope of the LX60 line.

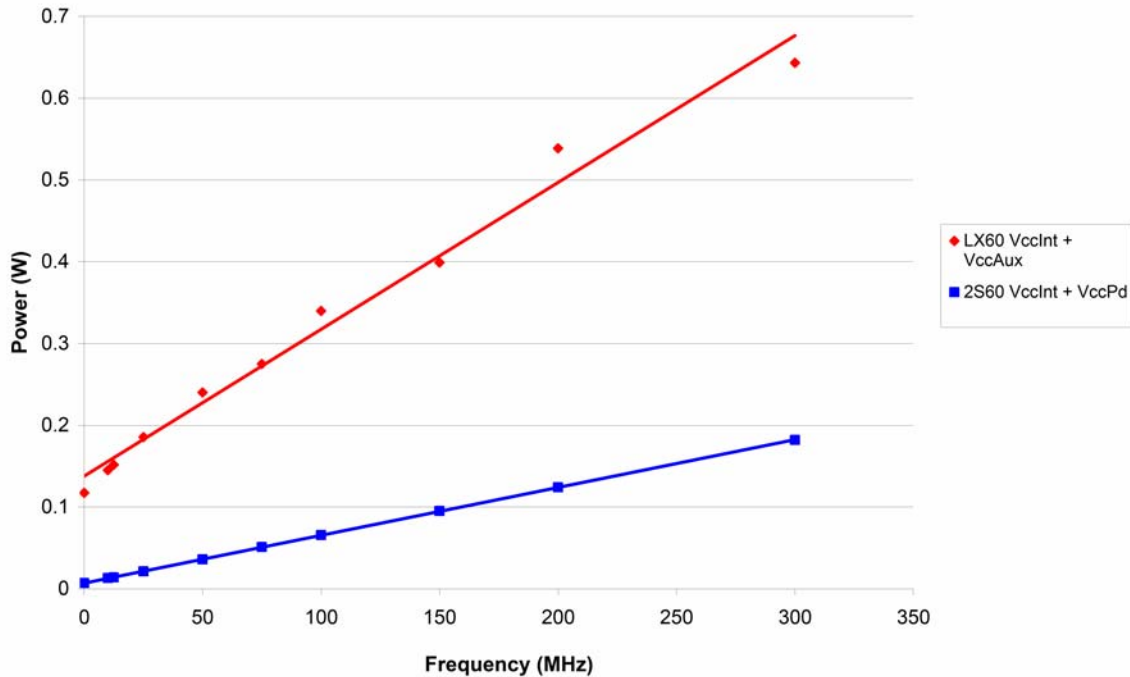


Figure 6. Bench-Measured PLL/DCM Power Comparison (Four Instances), Unconfigured Static Power Removed

Table 4 provides the PLL and DCM power results at 300 MHz, as well as the estimation error from the respective power analysis tools. As shown in Figure 6, the Stratix II PLLs consume one-fourth the power of the Virtex-4 DCMs. Quartus II PowerPlay power analyzer slightly over-estimates PLL power, while ISE XPower does not appear to model DCM power at all.

Table 4: Bench-Based PLL/DCM Power Comparison with Estimation Error

Design	Hardware Measured Dynamic Power (mW)			Estimation Error (“+” is Overestimate, “-” is Underestimate)	
	Stratix II EP2S60	Virtex-4 LX60	Stratix II to Virtex-4 Power Difference (%)	Quartus II PowerPlay Analyzer	ISE XPower
300 MHz, four PLL/ DCM	165 mW	684 mW	-76%	+3%	-100%

Fully Featured FPGA Designs

Two designs were used to measure the combined effect on power of all major components of both FPGAs. Beamforming is a NASA RADAR-imaging application that takes multiple channels of radar signal data, performs signal processing to compute focused beams, and then outputs the results on a lower-bandwidth output channel. The JPEG Encoder core converts supplied images into a JPEG-encoded images through DCT transformations. Both designs are architecture-independent HDL that employ logic, RAMs, and DSP. Neither was originally targetted at a Stratix II device.

Both designs were wrapped in random vector generation logic and measured on the bench. The results are shown in Table 5. The Stratix II implementations consume considerably less power – between four-fifths and one-half the power of the Virtex-4 implementations. Furthermore, the Quartus II PowerPlay power analyzer estimates power consumption to within 20% while XPower significantly underestimates power, underpredicting by a factor of 8× in the case of the JPEG Encoder!

Table 5: Bench-Based Measurement of Real-World Applications

Design	Hardware Measured Dynamic Power (mW/MHz)			Estimation Error (“+” is Overestimate, “-” is Underestimate)	
	Stratix II EP2S60	Virtex-4 LX60	Stratix II to Virtex-4 Power Difference (%)	Quartus II PowerPlay Analyzer	ISE XPower
Beamforming	4.50	8.45	-47%	13%	-55%
JPEG Encoder	10.68	13.32	-20%	3%	-86%

When these results are coupled with the customer logic-only results demonstrated in the Logic & Routing section, it is clear that Stratix II devices exhibit lower dynamic power for real-world designs.

Static Power

Static power is a component of total power that is independent of switching activity. The two causes of static power consumption are:

- Leakage paths from power to ground through inactive transistors. There are three sources of leakage currents, as shown in Figure 7: sub-threshold leakage, gate leakage, and drain-induced barrier leakage.. While all three currents become more significant as transistor dimensions shrink, sub-threshold leakage is the most significant for 90-nm devices at normal device operating conditions.
- Active power-ground paths. CMOS logic has no active power-to-ground path. Therefore, FPGAs consume very little static power due to these paths.

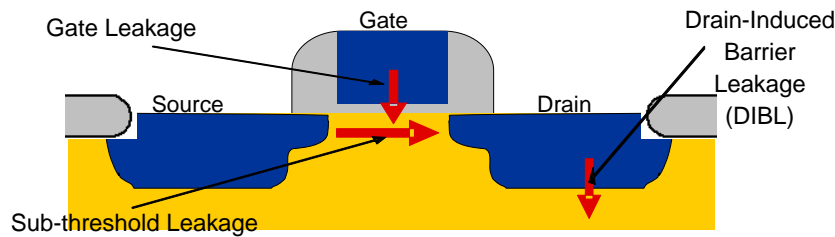


Figure 7. Leakage Currents in a CMOS Transistor

Sub-threshold leakage is caused by a small current that passes from source to drain even when a transistor is nominally off. Even when $V_{GS} = 0$ V (voltage between gate and source is zero), there is a small current present. This effect increases as transistor gate length and threshold voltage decrease, meaning sub-threshold leakage becomes more and more dominant in smaller process technologies. Therefore, with all other transistor parameters being the same, static power goes up for CMOS devices from 130 nm to 90 nm. Note that the manufacturer can vary other parameters to control static power (as both Altera and Xilinx do), but they all come with tradeoffs such as performance.

Sub-threshold leakage also increases exponentially as transistor junction temperature increases. The sub-threshold leakage of a device at 85° C can be up to 2.5× that of a device at 25° C. As a result, static power will vary as temperature varies, unlike dynamic power which is affected very little by temperature change.

Impact of Process Variation on Static Power

Sub-threshold leakage has an exponential dependence on critical process parameters such as transistor threshold voltage (a function of the transistor doping profile) and gate length. Many steps in silicon processing are stochastic, leading to a variation in the achieved values for these parameters. This results in die-to-die, wafer-to-wafer, and lot-to-lot variation in threshold voltages and gate lengths, and therefore variation in sub-threshold leakage. Because of this variation, manufacturer specifications are the only legitimate source of static power data.

Most FPGA power estimator tools come with maximum (worst-case) and typical specifications. These specifications represent what the device-to-device variation could be in static power. Typical represents the average unit, with 50% of the units consuming more static power. Worst-case should represent the FPGA specification for static power. In other words, the FPGA manufacturer is indicating that they test their FPGAs for this worst-case static power threshold. Altera recommends selecting maximum or worst-case when evaluating FPGA power.

One corollary of the impact of variation on sub-threshold voltage is that a single-unit measurement of static power is meaningless. The only expected result of such a measurement is that the device will fall within the worst-case specification. No other comparisons, such as one between the measured unit and the typical specification, are valid. Measurements across multiple units do not help either, since those devices may come from the same wafer or lot, or even have been produced near each other in time, and thus not be indicative of the true manufacturing process spread.

Static Power Comparison: Stratix II vs. Virtex-4

Each manufacturer's specifications (Stratix II early power estimator version 3.0, and Web Power Tool 7.1 for Virtex-4) were used to compare Stratix II and Virtex-4 static power consumption. Before comparing the static power of each device, it is important to understand how to construct a correct comparison.

Consider all significant voltage supplies – For each device, the reported static power is added across all power rails for an empty design. Both devices have a 1.2-V V_{CCINT} rail to power most of the core transistors. The Stratix II device has a V_{CCPD} (pre-drive) power rail used to power the I/O buffer pre-drivers. This rail operates at 3.3 V and has very little leakage power (up to 7 mA typical). Virtex-4 devices have a V_{CCAUX} 2.5-V rail that has significant leakage currents (up to 166 mA typical) and thus cannot be ignored. Both devices also have V_{CCIO} rails. The Stratix II device has minimal V_{CCIO} leakage (5 mA worst-case), while the specification for the Virtex-4 device has not been published. This white paper ignores the V_{CCIO} leakage for this comparison due to lack of data for Virtex-4 devices.

Use worst-case silicon specifications – When designing for static power, it is important to consider the worst-case silicon and the junction temperature your FPGA will be operating at (consider your ambient temperature with thermal resistance).

Compare devices with similar capacities –The Virtex-4 logic cell count is actually 12.5% higher than the number of logic cells in the parts. For example, the Virtex-4 LX200 actually has 178K 4-input LUTs and contains less logic than the Stratix II EP2S180, which contains the equivalent of 186K 4-input LUTs. For more background information on density comparisons and more on our logic density experiments refer to the *Stratix II vs. Virtex-4 Density Comparison White Paper*.

Table 6 shows a comparison of Stratix II and Virtex-4 static power for worst-case industrial silicon.

Table 6: Static Power Comparison, Stratix II vs. Virtex-4, Worst-Case Silicon

Stratix II (85°C Worst Case)				Virtex-4 (85°C Worst Case)			
Device	Power V_{CCINT}	Power V_{CCPD}	Total Static Power	Device	Power V_{CCINT}	Power V_{CCAUX}	Total Static Power
EP2S15	746 mW	10 mW	756 mW	LX15	276 mW	92 mW	368 mW
				LX25	462 mW	105 mW	567 mW
EP2S30	1.02 W	12 mW	1.04 W	LX40	726 mW	122 mW	848 W
EP2S60	1.90 W	17 mW	1.92 W	LX60	1.00 W	212 mW	1.21 W
				LX80	1.32 W	234 mW	1.55 W
EP2S90	2.70 W	22 mW	2.73 W	LX100	1.75 W	264 mW	2.02 W
EP2S130	3.77 W	29 mW	3.80 W	LX160	2.30 W	374 mW	2.68 W
EP2S180	4.75 W	37 mW	4.78 W	LX200	2.93 W	416 mW	3.35 W

The Xilinx V_{CCAUX} supply can account for up to 25% of its static power and is thus important to consider. Overall, Virtex-4 has a small static power advantage. However, this difference is outweighed by the Stratix II dynamic and I/O power advantage. To offset this difference even further, each Virtex-4 DCM adds 28 mW of static power when it is used in the design, compared to the Stratix II FPGA's PLL static power, which is 3 mW.

I/O Power

The I/O pins on an FPGA can dissipate a notable amount of power in addition to the core of the device. Like the core of the device, I/O pins have a static and dynamic component.

Dynamic power is drawn from three rails:

- V_{CCINT} for register and I/O selection logic
- V_{CCPD}/V_{CCAUX} for the I/O pre-driver circuitry
- V_{CCIO} for the output buffer

The V_{CCIO} power typically dominates, and the majority of current draw is due to the charging of internal and external capacitance. The internal pin capacitance due to the I/O buffer itself plus package can be significant, since FPGA I/O elements (IOEs) must contain support for many different I/O standards, and thus have a number of transistors attached to the I/O buffer. External capacitance arises from the PCB trace and the receiving device's pin and package capacitance.

In terminated I/O standards, there can be static current paths through the resistor divider networks, as shown in Figure 8. In the case of externally terminated standards, some of this current will be dissipated in off-chip resistors. Thus, some portion of the static power is not relevant to the *FPGA* thermal dissipation, but will be important for system thermal dissipation, and also for sizing the power-supply for the *FPGA* I/O rails, since this current is sourced from the *FPGA*.

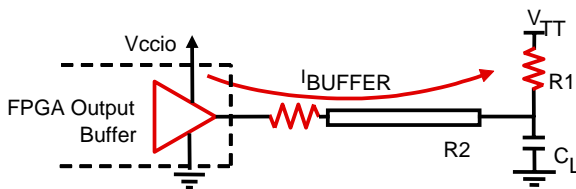


Figure 8. Static V_{CCIO} to V_{TT} Current for Terminated I/O Standards.

The Stratix II PowerPlay early power estimator and Quartus II PowerPlay power analyzer explicitly break-out I/O power into these various components, and report two power numbers: thermal power, which is dissipated on-chip, and supply current which is drawn from the V_{CCIO} rail(s).

Stratix II Power Optimization: Reduced Pin Capacitance

Stratix II devices employ a number of techniques to reduce I/O capacitance. Some of this capacitance reduction comes as a result of restricting some I/O standards to a subset of device I/O pins. For example, the left/right I/O pins were designed for high-speed LVDS, while the top/bottom I/O pins are the only ones with PCI clamp diodes.

Table 7 shows Stratix II and Virtex-4 measured pin capacitance, obtained via time-domain reflectometry. Stratix II IOEs have less than one half the pin capacitance. This translates to higher I/O speed, better edge rates and signal integrity margin, and lower I/O dynamic power. For lightly loaded non-terminated I/O standards, this will result in up to 50% power savings.

Table 7: TDR Measured Pin + Package Capacitance, Stratix and Virtex-4

I/O Type	Stratix II	Virtex-4
Left/Right	5.0 pF	12.5 pF
Top/Bottom	6.1 pF	12.5 pF

Tool-Based I/O Power Comparison

Figure 9 shows a comparison of Stratix II I/O power to Virtex-4 for a single output IOE running at 200 MHz (SDR) with a 10-pF load. The Stratix II results are taken from the early power estimator version 3.0, whose model is based on detailed SPICE simulations of I/O buffer schematics, including layout-extracted resistance and capacitance plus package trace information. This model is also validated against silicon across a range of I/O standards. The Virtex-4 results come from the Web Power Tool 7.1. The Stratix II thermal (on-chip) power is compared to the WPT reported total I/O power as Altera believes (based on first-principle calculations) that Xilinx does not include off-chip resistors in their power estimates.

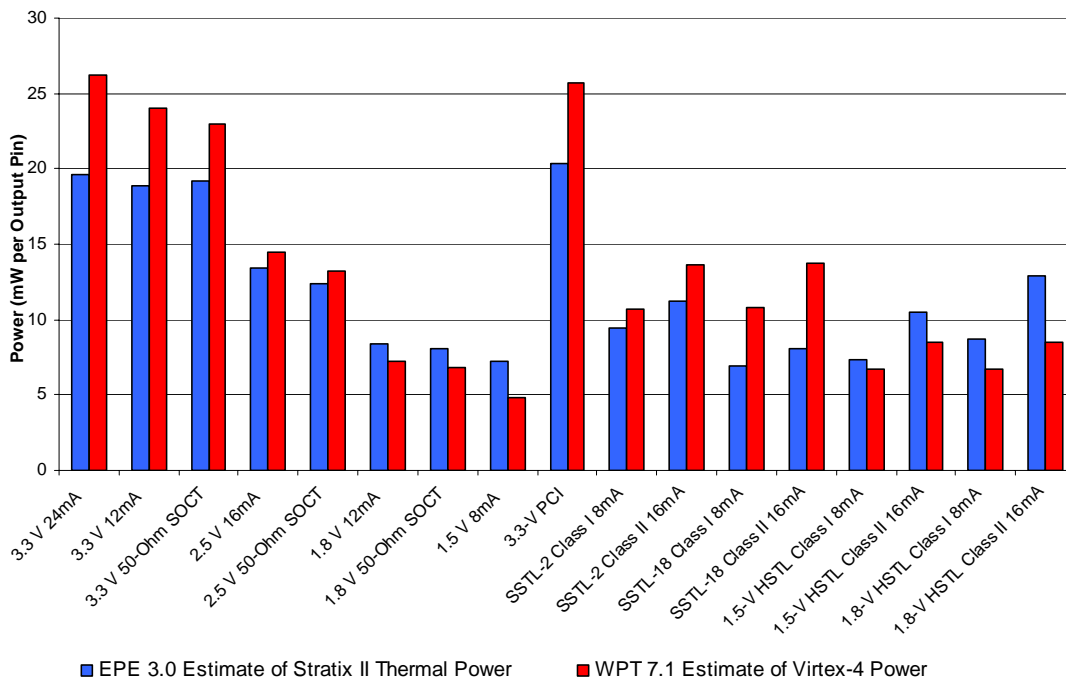


Figure 9. Estimator-Based Comparison of I/O Power, 200-MHz, Single-Data Rate, 10-pF Load

For most I/O standards, the Stratix II FPGA has a power advantage. For example, in LVTTTL and PCI, the Stratix II device consumes 20% less I/O power, owing to its lower pin capacitance. The two notable exceptions are 1.8-V/1.5-V LVCMOS and HSTL, where the Stratix II FPGA shows a small disadvantage.

Table 8 shows a comparison of Xilinx WPT estimated I/O power across a variety of Xilinx FPGA families ranging from the 180-nm Virtex-IIe to the 90-nm low-end Spartan-3 family and Virtex-4. In many cases the estimated power is identical down to the fourth digit of accuracy. While IOEs do not scale with process the same way core circuits do, it is beyond reason to believe that the IOEs on these devices consume

exactly the same power. It is clear that Virtex-4 I/O models are not simulation or silicon based. To contrast this data with Altera I/O power models, see Table 9.

Table 8: Xilinx I/O Power Models Across Devices

I/O Standard	Virtex-4 WPT 7.1	Virtex-II Pro WPT 4.0	Virtex-II WPT 4.0	Spartan-3 WPT 4.0
LVTTL 24 mA	2,614	2,614	2,723	2,614
LVTTL 12 mA	2,396	2,396	2,505	2,396
3.3-V LVDCI (50)	2,402	2,402	2,946	2,402
SSTL-18 class I	1,073	1,073	1,073	1,061
SSTL-18 class II	1,364	1,364	1,364	
1.8-V HSTL class II	845	845	855	845
PCI 66	2,559	2,559	2,668	2,559

Table 9: Altera I/O Power Models Across Devices

I/O Standard	Stratix II Early Power Estimator Version 3.0	Cyclone II Early Power Estimator Version 1.0	MAX II Early Power Estimator Version 3.0
LVTTL 24 mA	1,966	2,113	1,762
LVTTL 12 mA	1,968	1,983	1,646
3.3-V LVDCI with SOCT	2,137	2,060	N/A
SSTL-18 class I	707	445	N/A
SSTL-18 class II	841	545	N/A
1.8-V HSTL class II	1,280	936	N/A
PCI 66	2,039	1,816	1,924

Bench-based I/O Power Comparison

To validate the estimations of these tools, IOEs were measured on the bench using pseudo-random bit-streams, using the power test board. The board traces for both devices were matched in length and have identical characteristic impedance and capacitance, since both the EP2S60 and LX60 devices reside on the same (but electrically isolated) board.

Figure 10 shows the measured I/O supply power ($V_{CCIO} + V_{CCPD}/V_{CCAUX}$) consumption for 54 3.3-V 12-mA LVTTL outputs driving 54 LVTTL input pins. LVTTL power is dominated by the charging and discharging of pin, package, and external capacitance. The Stratix II I/O pins consume 35% less power than those on Virtex-4, highlighting the pin-capacitance advantage of this device.

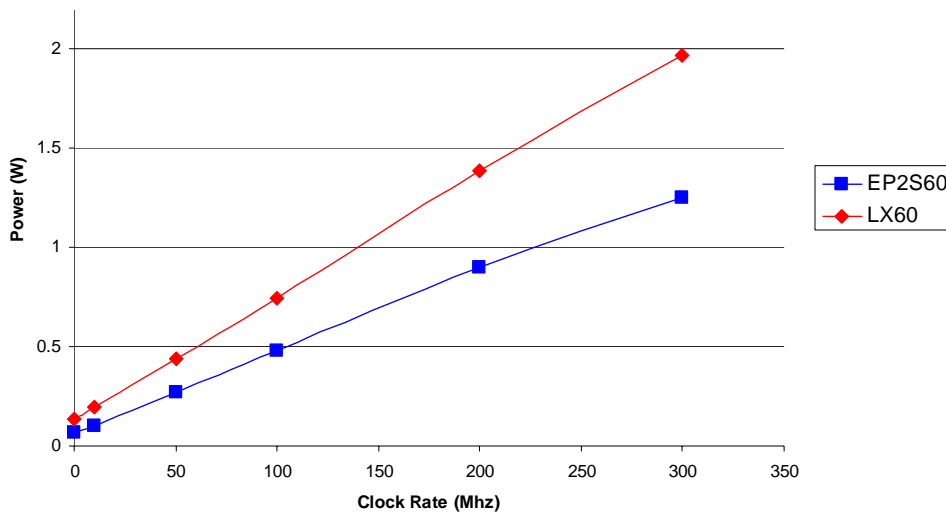


Figure 10. Bench Measured Power Comparison of 54 3.3V 12 mA LVTTTL Loop-Back I/O Pins

Figure 11 shows the measured I/O supply power ($V_{ccIO} + V_{ccPd/Aux}$) consumption for 128 single-ended 1.8-V HSTL Class II I/O pins. The Virtex-4 drive strength is the default (and only) value provided by the software, which, according to the spec, is 16 mA. This result shows that contrary to the tool estimations, the Stratix II device has an advantage in HSTL power.

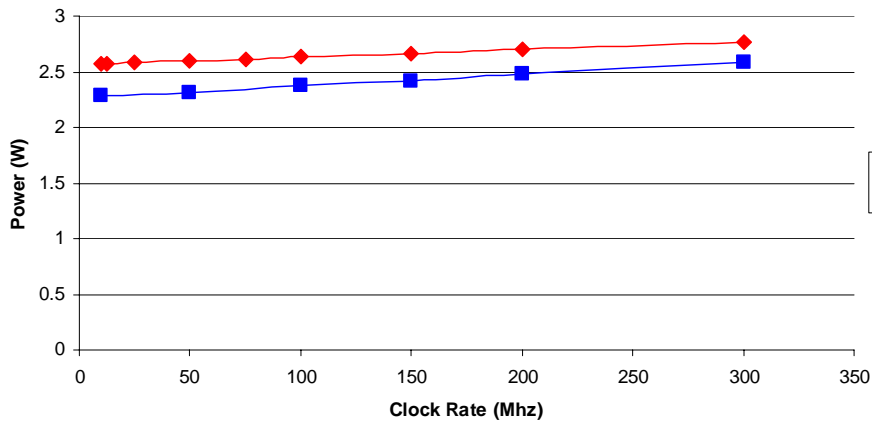


Figure 11. Bench Measured Power Comparison of 128 1.8V HSTL Class II I/O Pins

Total Power

When analyzing total power for a complete user design for Virtex-4 and Stratix II FPGAs, all three components of power should be considered: static power, dynamic power, and I/O power. While it is important to measure total power for your specific design, experiments using our design database indicate

that total power consumption in the typical design will be equal or better in Stratix II FPGAs. Benchmarks from 99 real-world designs show that dynamic power is responsible for 67% of total device power on average. Comparatively, static power and I/O power are responsible for 21.7% and 11.2%, respectively, for total device power. The dominant component of total device power is dynamic power and, therefore, the dynamic power advantage that Stratix II FPGAs have will easily negate any Virtex-4 static power advantage.

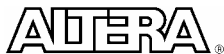
Conclusion

The white paper has provided hardware measured power consumption data for Stratix II and Virtex-4 FPGAs and also compared those measured to the power estimates made by each vendors power estimation tools. The following two points can be concluded from this data.

- Altera's Quartus[®] II PowerPlay power analyzer tool is accurate (to within 20%), while Xilinx's tools are significantly less accurate.
- Stratix II devices exhibit lower dynamic power over Virtex-4 devices, resulting in total device power that is equal.

While having lower total device power is generally desirable, having accurate power estimation tools is just as vital. There are two important reasons to utilize accurate power estimation tools:

- Avoid changes late in the design and prototyping phase. Inaccurate estimates can be costly and cause design issues, including: board re-layout, changes to power-management circuitry, changes cooling solution, unreliable FPGA operation, undue heating of other components, and changes to the FPGA design.
- FPGA CAD software that has accurate power models can perform better power optimizations during the design compilation process. Just as these tools can optimize for timing and area, they can also optimize for power. For the tool to make correct decisions during optimization an accurate power model is required.



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