



JPEG-E

Baseline JPEG Encoder Megafunction

Implements a high-performance image encoder that complies with the baseline ISO/IEC 10918-1 JPEG standard.

One of the fastest available JPEG megafunctions, the JPEG-E provides a high-performance solution for a variety of image and video compression applications. It can, for example, encode over 30 frames/sec for 4:3 HDTV, 1440x1152, 4:2:0.

In addition to processing baseline JPEG streams, the megafunction can compress non-standard motion JPEG streams. It can also be enhanced with an optional add-on bit-rate control block, which may benefit applications that have tight bandwidth constraints.

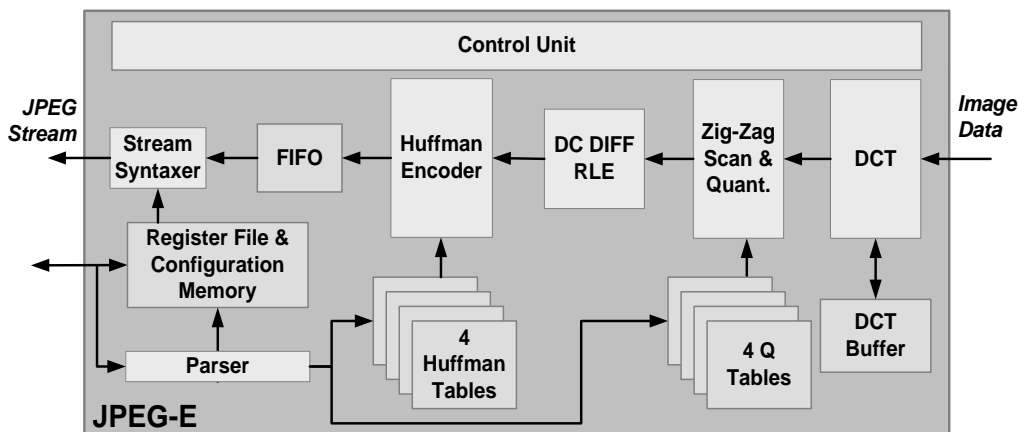
The megafunction includes FIFO-like pixel and stream input/output interfaces. Other standard interfaces (e.g. AMBA) are available. The megafunction is designed for reliability and ease of integration, and has been proven in a number of ASIC and FPGA designs. The deliverables include a software bit-accurate model that facilitates system on chip verification.

Applications

The high-performance JPEG-E megafunction is suitable for implementing a variety of multimedia applications, including:

- Digital cameras and camcorders
- Office automation equipment (multifunction printers, scanners, digital copiers etc)
- Medical imaging systems
- Video production suites
- Video conference and display-projection systems
- Surveillance systems

Block Diagram



Features

Baseline ISO/IEC 10918-1 JPEG Compliance

- Programmable Huffman Tables (two DC, two AC) and
- Programmable quantization tables (four)
- Up to four color components (optionally extendable to 255 components)
- Supports all possible scan configurations and all JPEG formats for input/output data
- Supports any image size up to 64k x 64k
- Supports DNL and restart markers

Additional Image Processing Capabilities

- Motion JPEG encoding/decoding
- Rate-Control (optional)

Designed for Easy Integration

- Single clock per input sample for encoding
- Fully programmable through standard JPEG stream marker segments
- Automatic headers generation
- Automatic program-once encode-many operation

Designed for High Quality

- Robust verification environment includes bit-accurate software model
- ASIC and FPGA proven in multiple designs
- Scan-ready design architecture
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)

Functional Description

The JPEG-E is configured by feeding it with JPEG headers, which contain table specification, image format, and encoding options data. The megafunction's configuration can be modified after the encoding of one or multiple frames. Image samples in any color space format is input to the JPEG-E in a MCU block by MCU block, raster scan order.

Consuming a single clock cycle per image sample, the JPEG-E can address the most demanding frame-based video compression applications. The JPEG-E outputs a complete JPEG-compliant data stream, including JPEG headers, the size of which can be dynamically controlled if the optional rate-control block is used.

Implementation Results

JPEG-E reference designs have been evaluated in a variety of technologies. The following Altera results are obtained after speed optimization during synthesis and place and route, while assuming that all megafunction I/Os are routed off-chip.

Altera Device	Logic	Frequency	Special Features	Quartus Version
Cyclone EP1C12-C6	7,201 LEs	125 MHz	9 M4K	7.1
Cyclone-II EP2C20-C6	5,337 LEs	154 MHz	9 M4K 19 DSP	7.1
Cyclone-III EP3C16-C6	5,259 LEs	161 MHz	9 M4K 19 DSP	7.1
Stratix EP1S10-C5	5,389 LEs	143 MHz	8 M4K / 1 M512 18 DSP	7.1
Stratix-II EP2S15-C3	4,519 ALUTs	229 MHz	8 M4K / 1 M512 18 DSP	7.1
Stratix-III EP3S50-C2	4,429 ALUTs	250 MHz	7 M9K / 15 DSP	7.1
Hardcopy-II HC210	53,310 HCELLs	238 MHz	9 M4K 18 DSP	7.1

Support

The megafunction as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The megafunction has been verified through extensive simulation and rigorous code coverage measurements. It has also been embedded in several products, and is proven in both ASIC and FPGA technologies.

Deliverables

The megafunction is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Altera version includes:

- Post-synthesis EDIF netlist
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)
- Simulation script, vectors, expected results, and comparison utility
- Software (C++) Bit-Accurate Model
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide