JPEG-D

Baseline JPEG Decoder Megafunction

Implements a high-performance image or video decoder that complies with the baseline ISO/IEC 10918-1 JPEG standard.

One of the fastest available JPEG megafunctions, the JPEG-D provides a high-performance solution for a variety of image and video decompression applications. It can, for example, decode 16:9 HDTV, 1920x1152, 4:2:0.

In addition to processing baseline JPEG streams, the megafunction can decompress non-standard motion JPEG streams. It can also be enhanced with an optional IDCT block that enables down-scaling in the frequency domain, a feature that allows decompression at various resolutions from the same compressed stream.

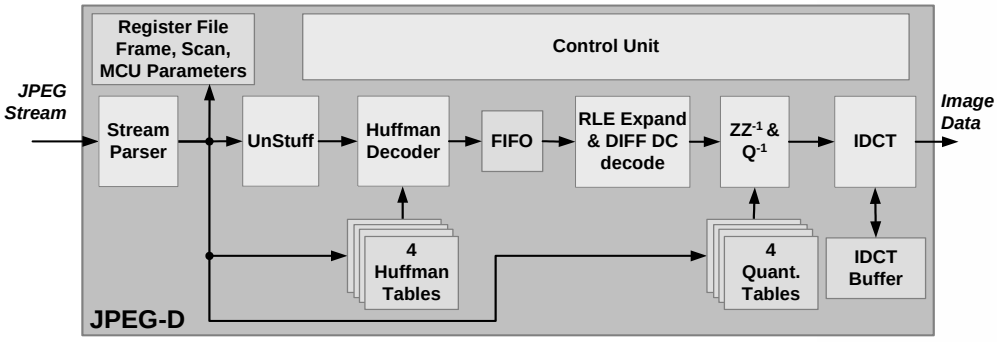
The megafunction includes FIFO-like pixel and stream input/output interfaces, and other standard interfaces (e.g. AMBA) are also available. The megafunction is designed for reliability and ease of integration, and has been proven in a number of ASIC and FPGA designs. The deliverables include a software bit-accurate model that facilitates system on chip verification.

Applications

The high-performance JPEG-D megafunction is suitable for implementing a variety of multimedia applications, including:

- Digital cameras and camcorders
- Office automation equipment (multifunction printers, scanners, digital copiers etc)
- Medical imaging systems
- Video production suites
- Video conference and display-projection systems
- Surveillance systems

Block Diagram



Features

Baseline ISO/IEC 10918-1 JPEG Compliance

- Programmable Huffman Tables (two DC, two AC) and
- Programmable quantization tables (four)
- Up to four color components (optionally extendable to 255 components)
- Supports all possible scan configurations and all JPEG formats for input/output data
- Supports any image size up to 64k x 64k
- Supports DNL and restart markers

Additional Image Processing Capabilities

- Motion JPEG decoding
- Decompressing at various resolutions via downscaling in the frequency domain (optional)

Designed for Easy Integration

- Stand alone operation
- Automatic self-programming by JPEG stream headers parsing
- Header errors catching
- Broadcasting of decoded image parameters for controlling peripherals such as a raster to block converter

Designed for High Quality

- Robust verification environment includes bit-accurate software model
- ASIC and FPGA proven in multiple designs
- Scan-ready design architecture

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Functional Description

The decoding path is highly autonomous, since the JPEG-D is self-configured (with table, image format and encoding options) by parsing the incoming JPEG stream's headers. The megafunction parses and checks all JPEG marker segments and signals in case it detects an error. Decoded image parameters are made available for controlling peripherals such as a block-to-raster converter.

Designed for continuous data flow, the JPEG-D can address the most demanding frame-based video decompression applications. Optional decoding at various resolutions from the same JPEG data-stream without the need for any extra buffering is enabled when the IDCT block is configured during synthesis to support downscaling in the frequency domain.

Implementation Results

JPEG-D reference designs have been evaluated in a variety of technologies. The following sample Altera results are obtained after speed optimization during synthesis and place and route, while assuming that all megafunction I/Os are routed off-chip.

Altera Device	Logic	Frequency	Special Features
Apex 20KE EP20K400E-1	8,849 LEs	60 MHz	16 ESB
Apex-II EP2A15-C7	8,912 LEs	80 MHz	11 ESB
Cyclone EP1C12-C6	8,796 LEs	85 MHz	7 M4K
Cyclone-II EP2C8-C6	6,796 LEs	112 MHz	7 M4K 19 DSP
Stratix EP1S10-C5	6,158 LEs	95 MHz	7 M4K / 1 M512 18 DSP
Stratix-II EP2S15-C3	6,053 ALUTs	140 MHz	7 M4K / 1 M512 18 DSP
Hardcopy-II HC210	55,220 HCELLs	192 MHz	12 M4K 36 DSP

Support

The megafunction as delivered is warranted against defects for three years from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The megafunction has been verified through extensive simulation and rigorous code coverage measurements. It has also been embedded in several products, and is proven in both ASIC and FPGA technologies.

Deliverables

The megafunction is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Altera version includes:

- Post-synthesis EDIF netlist
- Sophisticated HDL Testbench
- Simulation script, vectors, expected results, and comparison utility
- Software (C++) Bit-Accurate Model
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide

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Alma Technologies
This megafunction developed by the multimedia experts at Alma Technologies S.A.