



DI2CM

I²C Bus Interface - Master

ver 1.05

OVERVIEW

The DI2CM provides an interface between a microprocessor and an I²C bus. It can be programmed to operate with arbitration and clock synchronization to allow it to operate in multi-master systems.

- ◆ Allows operation from a wide range of input clock frequencies (build-in 8-bit timer)
- ◆ User-defined timing
- ◆ Fully synthesizable, static synchronous design with no internal tri-states

APPLICATIONS

- ◆ Embedded microprocessor boards
- ◆ Consumer and professional audio/video
- ◆ Home and automotive radio

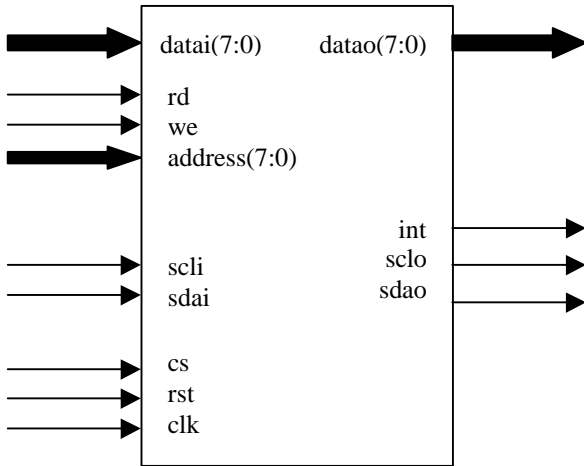
DELIVERABLES

- ◆ VHDL, Verilog source code
- ◆ VITAL simulation model
- ◆ HDL test bench
- ◆ Synthesis scripts
- ◆ Technical documentation
- ◆ Technical support

KEY FEATURES

- ◆ Master operation
- ◆ Multi-master systems supported
- ◆ Performs arbitration and clock synchronization
- ◆ Interrupt generation
- ◆ Supports speeds up to 3.4 Mbits/s (Standard, Fast and HS mode)

SYMBOL



PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
rst	input	Global reset
address(7:0)	input	Processor address lines
cs	input	Chip select
we	input	Processor write strobe
rd	input	Processor read strobe
scli	input	I ² C bus clock line (input)
sdai	input	I ² C bus data line (input)
datai(7:0)	input	Processor data bus (input)
datao(7:0)	output	Processor data bus (output)
sclo	output	I ² C bus clock line (output)
sdao	output	I ² C bus data line (output)
int	output	Processor interrupt line

PERFORMANCE

The following table gives a survey about the DI2CM performance in ALTERA® devices after Place & Route:

a) FLEX™ 10K30E-1

Area - 319 LC
System clock f_{max} - 106 MHz

b) APEX™ 20K60E-1

Area - 338 LC
System clock f_{max} - 109 MHz

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c) ACEX™ 1K10-1

Area - 319 LC
System clock f_{max} - 111 MHz

MODIFICATIONS

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