



EP510 CompactFlash Controller

Product Summary

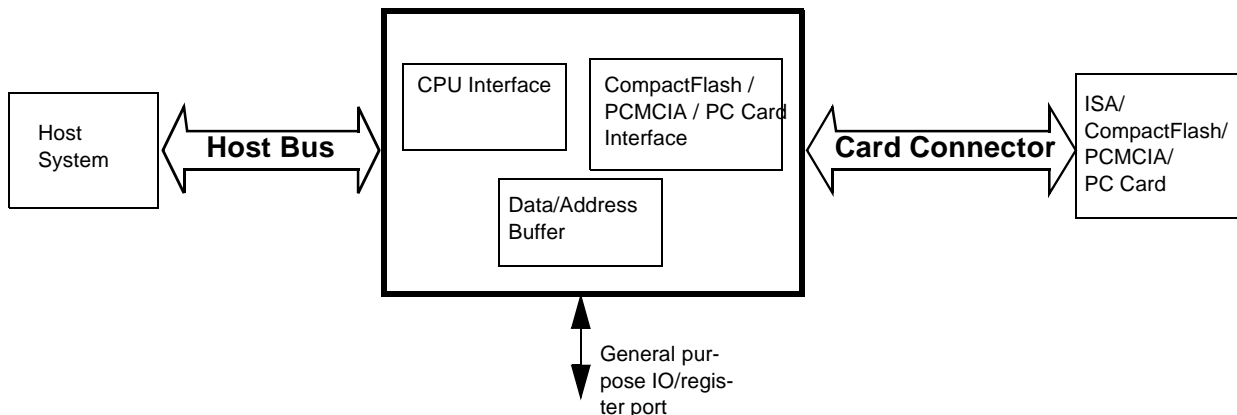
FEATURES

- Compliant to ISA bus, CompactFlash specification and PC Card/PCMCIA standards.
- Allows host bus devices to access ISA bus, CompactFlash, PC Card/PCMCIA devices.
- Different user interface options to support various CPU's including I960, X-86, PowerPC, MPC860, ARM, SH2/3/4 microprocessors.
- In PC Card/PCMCIA mode, supports attribute memory access, common memory access and IO access.
- In CompactFlash mode, supports attribute memory access, common memory access, IO access and IDE mode access.
- Converts 32-bit CPU access to multiple 8-bit or 16-bit accesses.
- Direct mapping of host address space to card address space.
- General purpose IO/register port.
- Designed for ASIC and PLD implementations.
- Fully static design with edge triggered flip-flops.
- Internal clock frequency at 33Mhz.

FUNCTIONAL DESCRIPTION

The host adapter allows host CPU or other devices residing on the CPU bus to access the PC Card/PCMCIA and CompactFlash cards. Different options of host bus interface is available to support different CPU such as ARM, PowerPC, SH and the I960.

The host adapter supports all four access types as defined in the PC Card/PCMCIA/CompactFlash standards, including memory and IO access for ISA bus, common memory, attribute memory and IO access for PC Card/PCMCIA/CompactFlash, and True IDE mode in CompactFlash. Different chip select signal





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is provided for the CPU or user logic to select the address space being accessed. In addition to the four address decoding for the four access types, the host adapter can decode one additional address space for general purpose I/O or register access through a separate port.

The CPU interface is 32-bit while the card interface can be either 8-bit or 16-bit. When the CPU request reading of 32-bit of data from the card, the host adapter performs multiple 8-bit or 16-bit read operation to collect 32-bit data for the CPU. When the CPU writes 32-bit data to the card, the host adapter performs multiple 8-bit or 16-bit write to the card to write all the data. Burst access support by the host adapter is optional.

Direct address mapping is provided by the host adapter with address space selected by chip select input signals. Customized address translation scheme can be provided upon customer request.

The host adapter operates based on the CPU bus clock. Its internal operation is based on the CPU bus clock edge. Because card interface normally operates at lower frequency than the CPU bus, the card interface signals are generated based on an internal clock which runs at a fraction of the CPU bus clock frequency. For example, if the CPU clock runs at 66Mhz, the clock ration of 8:1 can be used to operate the card interface at 8.33Mhz. The clock ratio is specified by the user logic during run time.

OPTIONAL FEATURES

The EP510 card controller supports the following optional features per customer specification

Types of CPU interface: ARM, I960, PowerPC, SH
Address translation
Additional I/O or register address space decoding
Burst access
CPU interface and card interface clock ratio