



# EC300 PCI Bus Arbiter

## Product Summary

### FEATURES

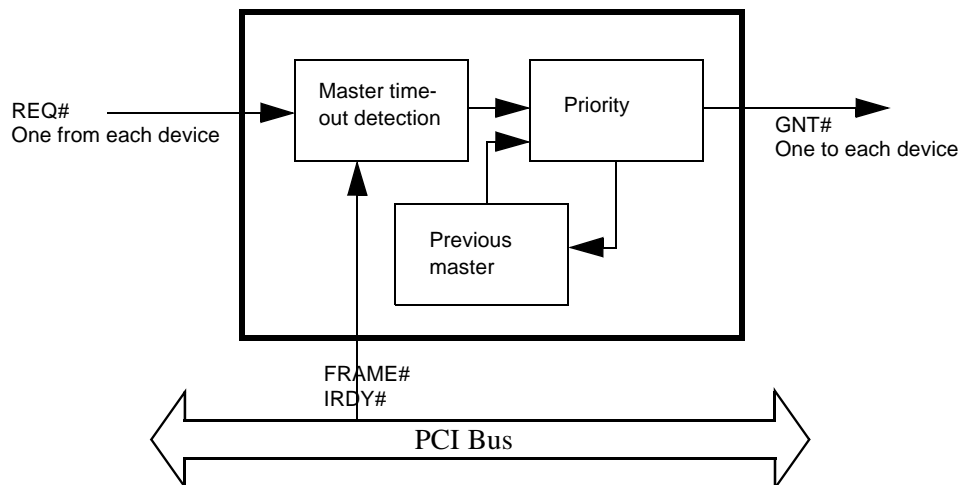
- Compliant with PCI bus specification 2.2.
- Designed for ASIC and PLD implementations in various system environments.
- Fully static design with edge triggered flip-flops.
- Supports two to any number of bus masters.
- Choice between rotating priority or fixed priority scheme.
- Bus parking.
- Supports both 32-bit and 64-bit PCI bus.
- Fast request-to-grant turn around time.
- Quiet cycle during master switch.
- Master time-out.

### DESCRIPTIONS

The EC300 PCI bus arbiter performs bus arbitration among multiple masters on the PCI bus. Up to any number of bus masters can reside on the PCI bus and request for the bus. One pair of request and grant signals is dedicated to each bus master.

When a bus master requires to initiate a bus transaction, it asserts the bus request signal, REQ# to the arbiter. There is a dedicated REQ# signal from each master to the arbiter. Based on the priority of the requests, the arbiter grants the bus to the master by asserting its GNT# signal. The arbiter implements bus parking, which means that if none of the bus masters request the bus, a bus grant will still be issued to one of the bus masters. The bus master which receives the parked bus grant can start using the bus without asserting bus request.

The EC300 implements either rotating priority or fixed priority scheme. In rotat-





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ing priority scheme, the requestor that was granted the bus most recently receives the lowest priority while the requestor position next to it receives the highest priority and the remaining requestor receives subsequently lower priority based on their position.

### OPTIONAL FEATURES

The following table summarizes the optional features which are provided with the core as required by user application.

Options	Description
Port size	Supports between 2 to any number of PCI masters on the same bus.
Priority scheme	Fixed or rotating priority