



EC240 64-bit PCI Bus Master/Target

Product Summary

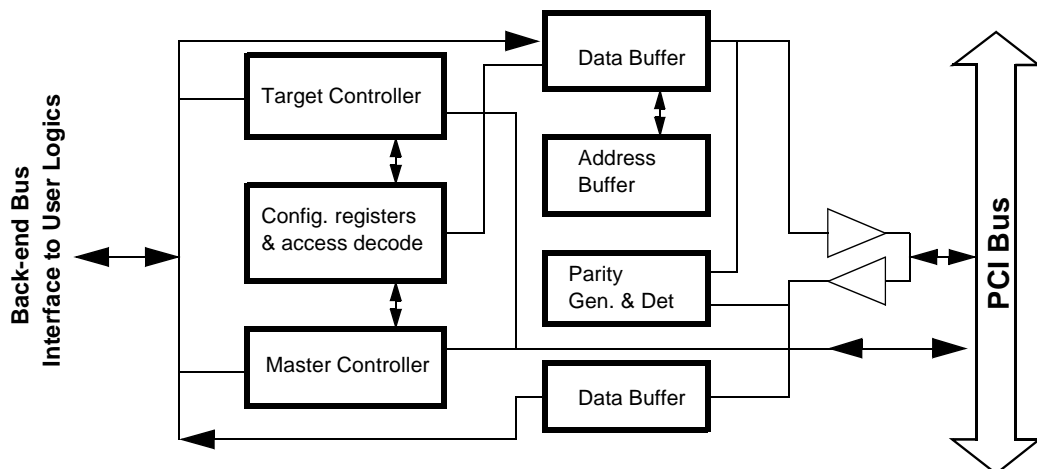
FEATURES

- Fully supports PCI specification 2.1 and 2.2 protocol.
- Supports both 64-bit and 32-bit bus systems.
- Supports dual address cycle (DAC) 64-bit addressing.
- Designed for ASIC and PLD implementations.
- Fully static design with edge triggered flip-flops.
- Combined bus master and target functions.
- Efficient back-end interface for different types of bus slave and master devices.
- Zero wait state burst data transfer.
- Automatic transfer restart on target retry and disconnect.
- High speed bus request and arbitration.
- Parity generation and parity error detection.
- Includes all PCI specific configuration registers.
- Optimized for devices with slow output enable control.

DESCRIPTIONS

The EC240 64-bit PCI bus Master/Target supports 32-bit and 64-bit bus systems. The back-end interface is a highly efficient and flexible back-end bus which provides for easy integration with other user logic. The core utilizes double data buffer design approach which minimizes design gate count and achieves highest possible data bandwidth at the same time.

The PCI bus master controller is capable of initiating memory or IO read and write upon back-end requests. The type of command and the burst size are specified by the user for each data transaction. Dual address cycle (DAC) is supported in accessing memories that reside above the 4GB address boundary. Once a master sequence begins, the core monitors the target device's signals on the PCI bus and the requested read or write operation is executed in compliance with the PCI specification.





EC240 64-bit PCI Bus Master/Target

The PCI target controller is capable of handling memory or IO read and write, DAC, and configuration read and write transactions. When a bus master on the PCI bus initiates a read or write transaction, the core decodes the address and the command and claims the transaction if the address is decoded to be within the address space of one of the target devices at the back-end. The PCI transaction is propagated to the proper target device in a simple protocol through the back-end bus.

The PCI target controller also responds to configuration read and write operations. The configuration accesses are processed automatically by the core without assistance from the user logic. All PCI specific configuration registers are supported in the 64-bit PCI Bus Master and Target core.

OPTIONAL FEATURES

The following table summarizes the optional features which can be provided with the core as required by user application.

Options	Description
Base address registers	Multiple base address registers, memory or IO mapped, and expansion ROM base address register.
Address and data multiplexing	Separate or combined back-end address and data buses.
DAC	Dual Address cycle to support 64-bit address space.
Direct FIFO interface	The back-end bus can be made to directly interface a FIFO.
Burst length	Supports any number of word transfer count bits for master transactions.
Target burst	Burst support for burst capable back-end target devices.
Target retry, disconnect, and abort	Support for back-end initiated target retry, disconnect and abort.
Asynchronous clock domains	Clock synchronization for PCI clock domain and asynchronous back-end clock domain.