



EC150 PCI-to-ISA Bridge

Product Summary

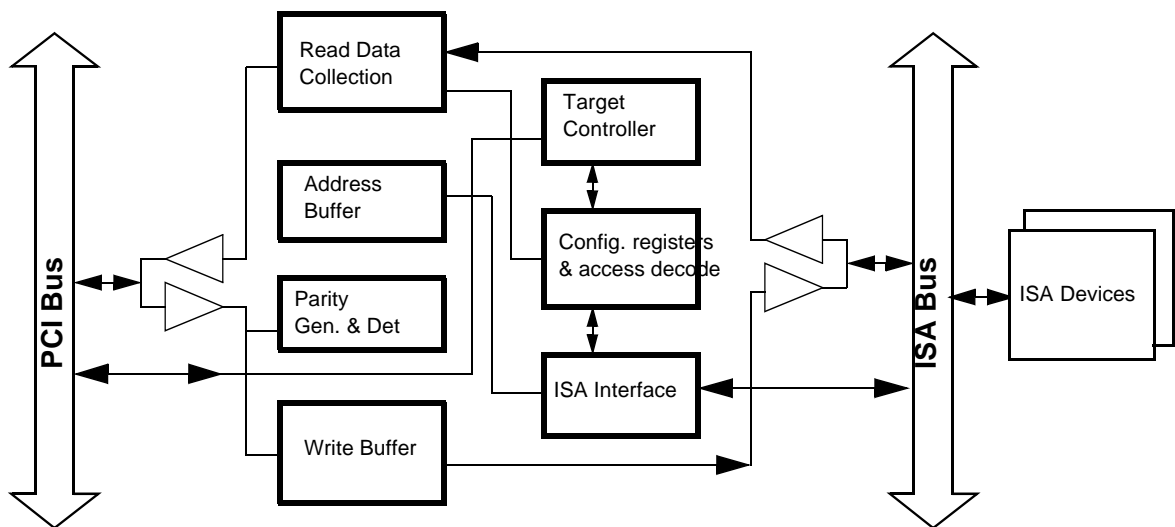
FEATURES

- PCI spec 2.1 and 2.2 compliant
- Convert PCI transaction to ISA bus transaction
- Function as PCI target on PCI bus
- Function as ISA master on ISA bus
- Map PCI address space to ISA address space through Base Address Register
- Supports 16-bit and 8-bit data transfer, memory and IO transfers on ISA bus
- ISA bus operates on one-fourth the frequency of the PCI clock
- Performs multiple ISA operations to transfer each 32-bit PCI word
- Write buffer to speed up PCI-to-ISA write transfer
- Support ISA devices with different speed by using NOWS# and CHRDY signals
- Parity generation and parity error detection on PCI bus.
- Includes all PCI specific configuration registers.
- Fully synchronous design, no gated clock or transparent latch. All flip-flops are rising edge trigger

DESCRIPTIONS

The EC150 is a bridge between the PCI bus and the ISA bus. It functions as a PCI target on the PCI bus. PCI transactions addressed to this target are forwarded to the ISA bus. If it is a read transfer, the core waits for all read data from the ISA slave and returns the data to the PCI bus. If it is a write transfer, the core post the write data to its internal write buffer, terminates the PCI bus, and then writes the data to the ISA slave.

With typical PCI bus running at 33Mhz, the EC150 operates the ISA bus at one-





EC150 PCI-to-ISA Bridge

fourth the frequency of the PCI bus. The ISA bus operates at 8.33Mhz.

Since the ISA bus is running at a much slower speed than the PCI bus, the core does not accept burst data from the PCI bus. Burst transfer on the PCI bus will require too many cycles to complete on the ISA bus. If the master attempts a burst transfer, the core issues disconnect with the first data so that it releases the PCI bus for other devices to transfer data.

The EC150 supports 8-bit and 16-bit ISA bus devices while the PCI bus is 32-bit wide. The core is capable of taking one PCI transfer and converting it into 4 or 2 transfers on the ISA bus. In the case of a 32-bit read, it performs multiple ISA reads to collect all 4 bytes of data and returns a 32-bit word to the PCI bus. In the case of 32-bit write, it performs multiple ISA writes to write out all 4 bytes to the ISA device.

The EC150 generates the ISA reference clock, BCLK, by dividing the PCI clock signal by four. All internal operations and input sampling of the core is performed by using the PCI clock. The design is done in such a way that it appears to ISA devices that the design is synchronous with BCLK.