



EP525 Pipeline SDRAM Controller

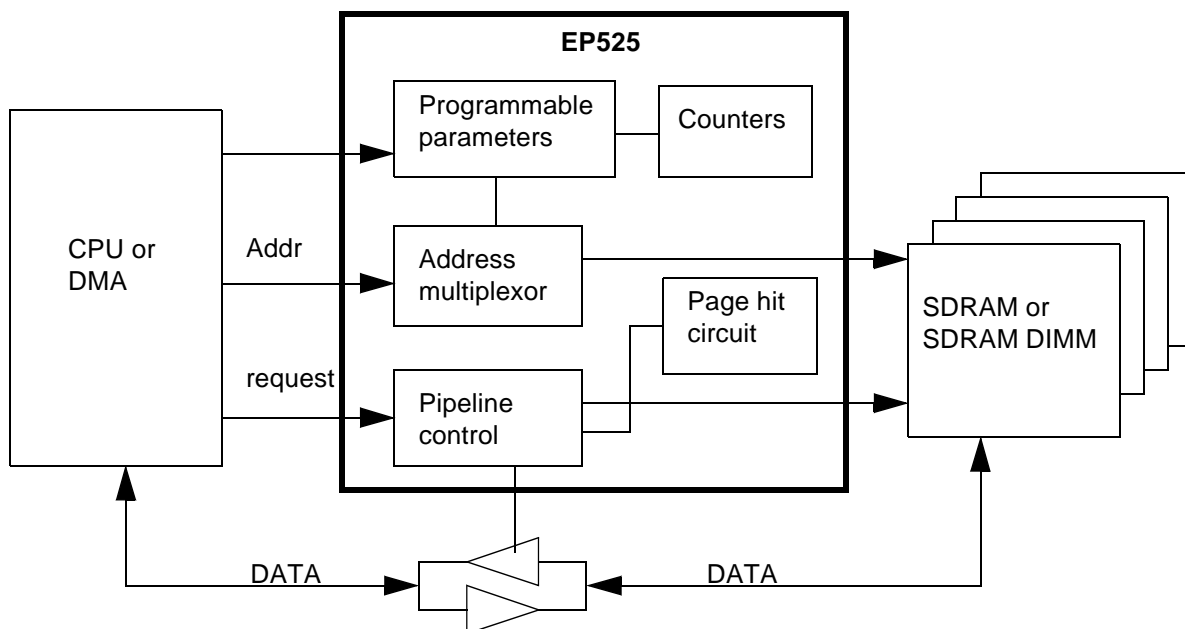
Product Summary

FEATURES

- Designed with synthesizable HDL for ASIC and PLD synthesis.
- Supports both discrete SDRAM chips and PC100/133 SDRAM DIMM.
- Supports register mode and non-register mode SDRAM DIMM.
- Supports industrial standard SDRAM from 64Mbit to 256Mbit device sizes.
- Pipeline access allows continues data transfer without wasted cycle.
- Supports column-only access on page hit.
- Programmable memory size: 4, 8, 16 and 32 bits per SDRAM.
- Programmable word size: 16, 32 and 64 bits.
- Supports all burst lengths: 1, 2, 4, 8 and full page.
- Zero wait state burst data transfer.
- Programmable SDRAM access timing parameters.
- Automatic refresh generation with programmable refresh intervals.
- Programmable memory configuration registers.
- Supports external data buffer between user device and SDRAM data bus by providing a transmit/receive signal.

DESCRIPTIONS

The EP525 pipeline SDRAM controller is a high performance SDRAM controller designed for transferring data to and from any industry standard SDRAMs or PC100/133 SDRAM DIMMs at the highest possible data rate. It interfaces between multiple SDRAM memory subsystem and a user interface. It performs SDRAM read and write accesses based on the user requests.





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The pipeline feature of the EP525 SDRAM controller allows the user to specify the next access address while the current data transfer is in progress. Multiple data transfers can be cascaded together to read or write data from the SDRAM continuously, without any wasted cycle between accesses.

Another performance enhancement features of the EP525 is that it allows column-only access for both read and write. The SDRAM controller keeps the previous accessed row open. If the new request hits the same row, a column access is performance thus eliminate row access time. The SDRAM controller simultaneously keeps track of four open rows, one for each bank.

The SDRAM controller can be programmed to support different sizes and configurations of SDRAMs. The SDRAM device sizes supported are 64Mbits, 128Mbits, and 256Mbits. The data width per SDRAM device can be programmed to 4, 8, 16 or 32 bits. The user can use multiple SDRAMs to build an wider memory subsystems.

The SDRAM controller is fully programmable. All access timing parameters such as CAS latency, row-to-column delay, refresh interval, etc., are programmable to support different speed grades of SDRAM devices and different operating frequencies. All the timing parameters can be modified during run-time by a separate access port. The timing parameters can also be set to the proper default values during compile time so that there is no need to program them during run-time.

The user interface of the SDRAM controller is a user-friendly synchronous bus, similar to the I960 microprocessor interface. The user provides the address for each access and the SDRAM controller automatically generate the row (RAS) and column (CAS) access cycles to transfer data. The user can specify single or burst data transfer. In burst data transfer, zero wait state data bursting is supported to maximize memory bandwidth. The SDRAM controller issues pre-charge command to terminate each access and periodically issues refresh commands to refresh the SDRAM devices.

OPTIONAL FEATURES

The EP525 SDRAM controller supports the following optional features per customer specification

ECC or parity support of memory data
Posted write buffers
Multiple request ports to access SDRAM