



# EP240 AHB Bus Master

## Product Summary

### FEATURES

- Supports AHB bus interface to the ARM CPU.
- User interface designed for high speed access to any slave devices on the AHB Bus.
- User specified single or burst data access on the AHB interface and user interface.
- Handles wait state insertion by any slave devices.
- Automatic bus arbitration.
- Supports all slave device responses: OKAY, RETRY, SPLIT and ERROR.
- No delay insertion on data transfer between user interface and AHB bus.
- Supports bus parking.
- Efficient user interface optimized for on-chip data communication.
- User interface matches seamlessly with Eureka Technology DMA controller or PCI bridge.
- Optimized for ASIC and PLD implementations, including Excalibur PLD.

### DESCRIPTIONS

The AHB bus master is an interface unit allowing user logic to initiate data transfer on the AHB bus. The user specifies the type of transaction to be executed on the AHB bus through a user-friendly interface. The bus master is optimized to interface with devices such as DMA and PCI bus bridge to initiate data transfer on the AHB bus.

Once the user request is received, the bus master automatically arbitrates for the AHB bus and executes the transaction on the AHB bus following the AHB bus protocol. Data received from the AHB bus is returned to the user interface with no delay.

All four types of slave responses and slave wait states are handled by the bus master. In the event of RETRY and SPLIT, the bus master automatically re-issues the transaction until all data are transferred.

### BLOCK DIAGRAM

