



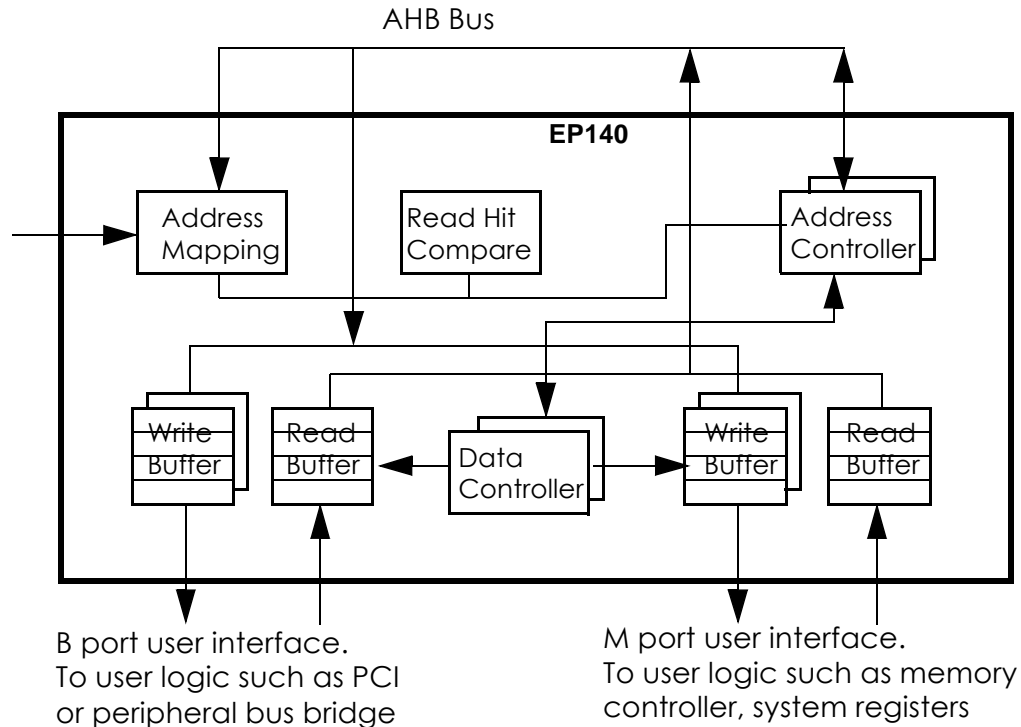
EP140 AHB Bus Slave

Product Summary

FEATURES

- Supports AHB bus interface to the ARM CPU.
- User interface designed for high speed access to two sets of on-chip or off-chip modules.
- Four write buffers to process posted write.
- Dual read buffers to process CPU read.
- Read access to external bus handled as delay read to avoid system deadlock.
- Supports burst transfer and zero wait state to maximize data bandwidth.
- Supports data width of 8, 16 and 32 bits.
- Supports burst transfers up to 16 data.
- Supports early burst termination and CPU master busy.
- Multiple bus slave is supported by Ready signal input and outputs.
- Programmable address mapping to multiple address spaces.
- User interface optimized to access secondary bus such as PCI and memory sub-systems based on SDRAM and FLASH.
- Optimized for ASIC and PLD implementations, including Excalibur PLD.

BLOCK DIAGRAM





EP140 AHB Bus Slave

DESCRIPTIONS

The EP140 is an AHB bus slave device designed to interface various user logic with the ARM CPU. It decodes the AHB address and dispatch the request to user logic through two user interface ports. The bus slave also regulates the data flow between all ports to optimize performance. Different user logic such as SDRAM controller, FLASH controller, PCI host bridge, DMA and UART can be connected to the AHB bus through the slave.

The EP140 is capable of simultaneously transferring data between the AHB bus and the two user interfaces. The B port user interface is optimized for peripheral bus controller access such as PCI bus access and the M port user interface is optimized for memory controller access. However, both user interface ports use a very simple and user-friendly protocol so that different types of user logic other than PCI and memory controller can be connected to either interface port.

The AHB bus slave contains 4 write buffers, two for each user interface. Each write buffer can store up to 64 bytes of data. The dual write buffer structure allows the CPU to post write data into one buffer while the user interface is extracting data from the other write buffer. Up to 4 different write commands can be posted into the AHB slave by the CPU while the write request is processed by the user logic.

Reading by the AHB bus can be handled as delay read or as real time read by the slave. Delay read method is suitable for interfacing with external bus such as PCI bus. Under this method, the AHB slave retries the CPU while it is reading data from the user logic. Instead of inserting wait state while waiting for return data, the AHB slave uses retry to free up the AHB bus for other accesses. Once read data is available, data is returned to the CPU with zero wait state in subsequent read. The primary benefit of the delay read method is to prevent deadlock between the external bus and the AHB bus.

The real-time read method is suitable for reading device that has small read latency such as SDRAM or other memory controller. The bus slave inserts wait state on the AHB while waiting for data to return from memory. No retry is issued so that data is returned to the CPU as soon as it arrives from memory.

The AHB bus slave contains two user interfaces and each interface contains its own set of write buffers to avoid sharing of the write buffers and read buffers and avoid resource dependence. The buffers also support CPU access using different data size from the user logic. The AHB bus slave supports data size of 8, 16 and 32-bit from the CPU while the user logic transfers data at 32-bit.