



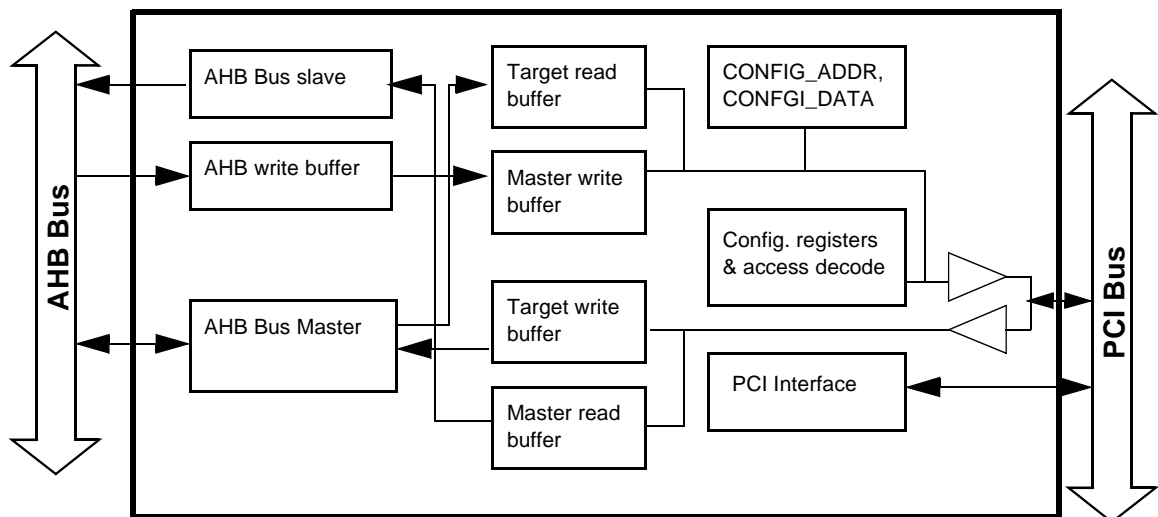
EP454 AHB-to-PCI Host Bridge

Product Summary

FEATURES

- Fully supports PCI specification 2.1 and 2.2 protocol.
- Supports AHB bus protocol.
- Downstream access transfer from AHB bus to PCI bus.
- Upstream access transfer from PCI bus to AHB bus.
- AHB bus and PCI bus operate at independent clock domains.
- Total of six write buffers for write data posting for all interfaces.
- Read access to PCI bus handled as delay read to prevent system deadlock.
- Supports AHB burst transfers up to 16 data.
- Supports all AHB slave response types when functioning as AHB bus master.
- PCI interface includes bus master, bus target and configuration access initiation.
- Generates standard PCI type 0 and type 1 configuration accesses.
- Supports early burst termination and CPU master busy.
- Automatic handling of configuration register read/write access.
- Supports target retry, disconnect, abort and wait state insertion.
- Parity generation and parity error detection.
- Includes all PCI specific configuration registers.
- Supports high speed bus request and bus parking.
- Optional PCI bus arbiter with fix, rotating, and custom priority.
- Optimized for ASIC and PLD implementations, including Excalibur PLD.

BLOCK DIAGRAM





EP454 AHB-to-PCI Host Bridge

DESCRIPTIONS

The EP454 PCI host bridge is designed for interfacing the ARM CPU with the PCI bus and forward data access from both the upstream and downstream directions. The host bridge consists of three functional units: AHB bus slave, AHB bus master, and PCI interface. The AHB bus and the PCI bus can operate at two different clock domains.

Any bus mastering devices on the AHB bus can also access the host bridge. The core has multiple data buffers to achieve high speed data posting, prevent bus deadlock, and allow clock domain crossing for the data.

The host bridge core allows the CPU to initialize the entire system during power-up reset using standard PCI protocol. Both type zero and type one transactions are supported. The CPU requests configuration access on the PCI bus by writing to or reading from the CONFIG_ADDR and CONFIG_DATA registers which are contained in the host bridge.

The host bridge initiates memory or IO read and write on the PCI bus upon AHB bus requests. It contains 4 write buffers, two in the AHB bus clock domain and two in the PCI clock domain, to post write data. Data can be written from the AHB bus at the same time write operation is running on the PCI bus.

Reading by the AHB bus is handled as delay read. The AHB slave retries the CPU while it is read data from the PCI bus. Instead of inserting wait state while waiting for return data, the AHB slave uses AHB bus retry to free up the AHB bus for other accesses. Once read data is read from the PCI bus, data returned to the CPU with zero wait state in subsequent read. The primary benefit of the delay read method is to prevent deadlock between the PCI bus and the AHB bus.

The host bridge functions as a PCI target when accessed by an external PCI bus master. The PCI target contains two write buffers and a read buffer to handle write posting and transfer data across the two clock domains. The request received from the PCI bus is forwarded upstream to the AHB bus through the built-in AHB bus master. When function as a AHB bus master, the host bridge supports all the bus slave response type, wait state insertion, and supports burst data transfer.