

## Features

- AMCC-compatible FlexBUS-3 Link Layer with FIFOs
- ATM and Packet Over SONET (POS) modes
- Single- and multi-link operation, scalable from 1 to 48 links
- Programmable per-port bandwidth allocation
- Direct/pollled cell/packet available modes
- Programmable FIFO size with programmable almost empty/almost full thresholds
- Programmable burst size
- Automatic link selection based on FIFO fill levels and cell/packet available information
- 32-bit data bus width
- Parity generation/checking
- Altera Atlantic Interface (Slave) on user's side.
- Full synchronous design, exceeds: Clk = 104 MHz
- Fully automatic test bench including driver/monitor
- Easy to use in Mux/Demux and bridge functions

## Standards Compliance

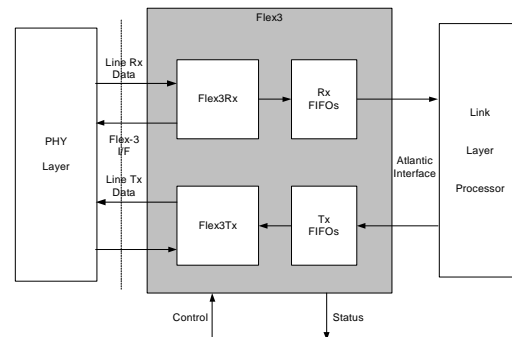
- AMCC FlexBUS-3

## Benefits

- Faster FPGA and ASIC development for improved time-to-market with FlexBUS-3 functions

- Lower development cost through design reuse
- Available source code licensing for easy design integration and migration to gate arrays or ASICs
- Ample design flexibility using control signals and generics/parameters
- Verified functionality and standards compliance

## Description



**Figure 1: FlexBUS-3 Link Layer Application**

The FlexBUS-3 interface allows the interconnection of Physical (PHY) Layer devices to Link Layer devices in 2.5 Gb/s Asynchronous Transfer Mode (ATM) and Packet Over SONET (POS) applications. Modelware's FlexBUS-3 Link Layer core performs the interface functions on the Link Layer side of the interface as shown in Figure 1.

The core interfaces to the Link Layer via Altera's Atlantic interface, and to the Physical Layer via the FlexBUS-3 interface (Figure 1). The Flex3Tx block monitors the Tx FIFOs fill levels and the Tx cell/packet available information received from the PHY Layer device. If a Tx FIFO has data and the cell/packet available information for the corresponding channel indicates that it is ready to accept data, the Flex3Tx block initiates a data transfer from the Tx FIFO to the PHY device.

The Flex3Rx block monitors the Rx FIFOs fill levels and the Rx cell/packet available information from the PHY device. If an Rx FIFO can accept a cell or packet burst and the cell/packet available information for the corresponding channel indicates that it is ready to send data, the Flex3Rx block initiates a data transfer from the PHY device to the Rx FIFO.

## Gate Count

The FlexBUS-3 Link Layer Core targeted to the APEX 20KE family uses:

### 4 Channels

Logic Elements (LEs): 3250

Embedded System Blocks (ESBs): 24

### 16 Channels

Logic Elements (LEs): 14000

Embedded System Blocks (ESBs): 100

## Design Package

The FlexBUS-3 Link Layer Core source code package contains:

- Source code or Netlist
- Test bench (source code option)
- Scripts and data files for simulation (behavioral, gate-level, and back-annotated), synthesis, and FPGA layout
- Detailed documentation:
  - Reference Guide: Core features, architecture, interfaces, and operation
  - User's Guide: Core simulation, synthesis, and FPGA layout step-by-step procedures.

## Supported Tools

- MTI Modelsim for simulation
- Exemplar Leonardo Spectrum for synthesis
- Altera Quartus

## Ordering Information

Modelware, Inc.

Tel: (732)936-1808

Fax: (732)936-1838

E-mail: sales@modelware.com

Internet: www.modelware.com

## Trademarks

Modelware is a registered trademark of Modelware, Inc.

Exemplar and Leonardo Spectrum are trademarks of Exemplar Logic, Inc.

Altera, Quartus, and Atlantic are trademarks of Altera Corporation.

FlexBUS is a trademark of AMCC.