

## 1 Introduction

Ethernet is available in different speeds (10/100/1000 and 10000Mbps) and provides connectivity to meet a wide range of needs from desktop to switches. MorethanIP IP solutions provide a solution for each Ethernet application with a library of configurable MAC (Media Access Control) and PCS (Physical Coding Sub-layer) Cores.

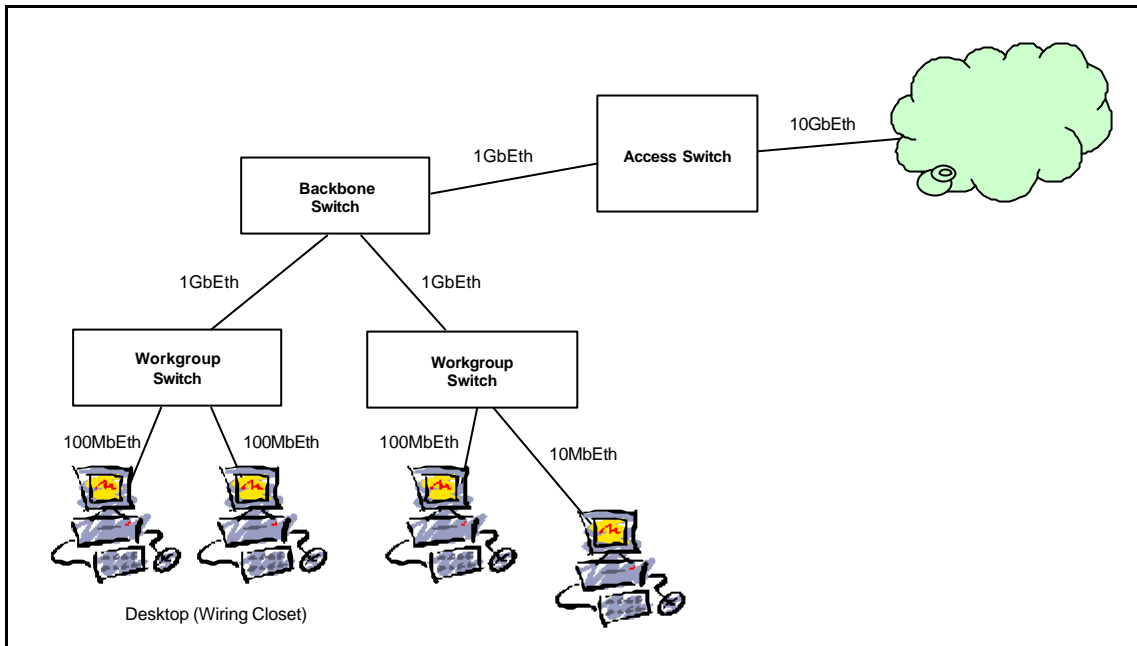


Figure 1: Enterprise LAN Topology Example

The MAC-NET Core implements, in conjunction with a triple speed 10/100/1000 MAC, network acceleration functions above Layer 2, which are designed to accelerate the processing of various common networking protocols such as IP, TCP, UDP and ICMP providing wire speed services to Client applications.

The Core implements a triple speed 10/100/1000Mbps Ethernet MAC compliant with the IEEE802.3-2002 standard. The MAC layer provides compatibility with Full Duplex Gigabit Ethernet LANs as well as Half- or Full-Duplex 10/100Mbps Ethernet and Fast Ethernet LANs.

The MAC operation is fully programmable and can be used in NIC (Network Interface Card), bridging or switching applications. For SNMP (Simple Network Management Protocol) the Controller implements Management Information Base (MIB, MIB-II) according to IETF RFC2665 and Remote Network Monitoring (RMON) according to IETF RFC 2819. All registers are accessible via a 32-Bit parallel interface.

The Core also implements a hardware acceleration block to optimize the performance of network controllers providing IP and TCP,UDP,ICMP protocol services. The acceleration block performs, critical functions, which are typically implemented with large software overhead.

The Core implements programmable embedded FIFOs that can provide, on the Receive path, buffering for loss-less flow control.

Advanced Power Management features are available with Magic Packet detection and programmable power down modes.

The Core provides a flexible and evolutive solution for a large number of applications such as SAN (Storage Area Network), NAS (Network Attached Storage), Enterprise File Servers, Firewalls, Gateways or Routers.

The core can seamlessly connect to any industry standard Gigabit Ethernet PHY device via a Gigabit Medium Independent Interface (GMII for 1000Mbps application) or Medium Independent Interface (MII for 10/100Mbps applications) and to a user application via the Avalon SOC (System on a Chip) bus interface which provides seamless connectivity to any Avalon based system.

Optionally, the Core implements an integrated 1000Base-X PCS and PMA for Gigabit only operation when implemented in Altera Stratix GX devices. Using Stratix GX embedded SERDES features provides a highly integrated solution reducing board complexity and system cost.

The MAC-NET core is fully integrated in the Altera SOPC builder for easy system integration and use. It includes supporting files for software development and drivers for a TCP/IP stack library.

The core is optionally delivered in generic synthesizable HDL code (For use in Altera CPLD or ASIC technologies), or as a CPLD netlist, which provides a lower cost solution.

## 2 Application Example

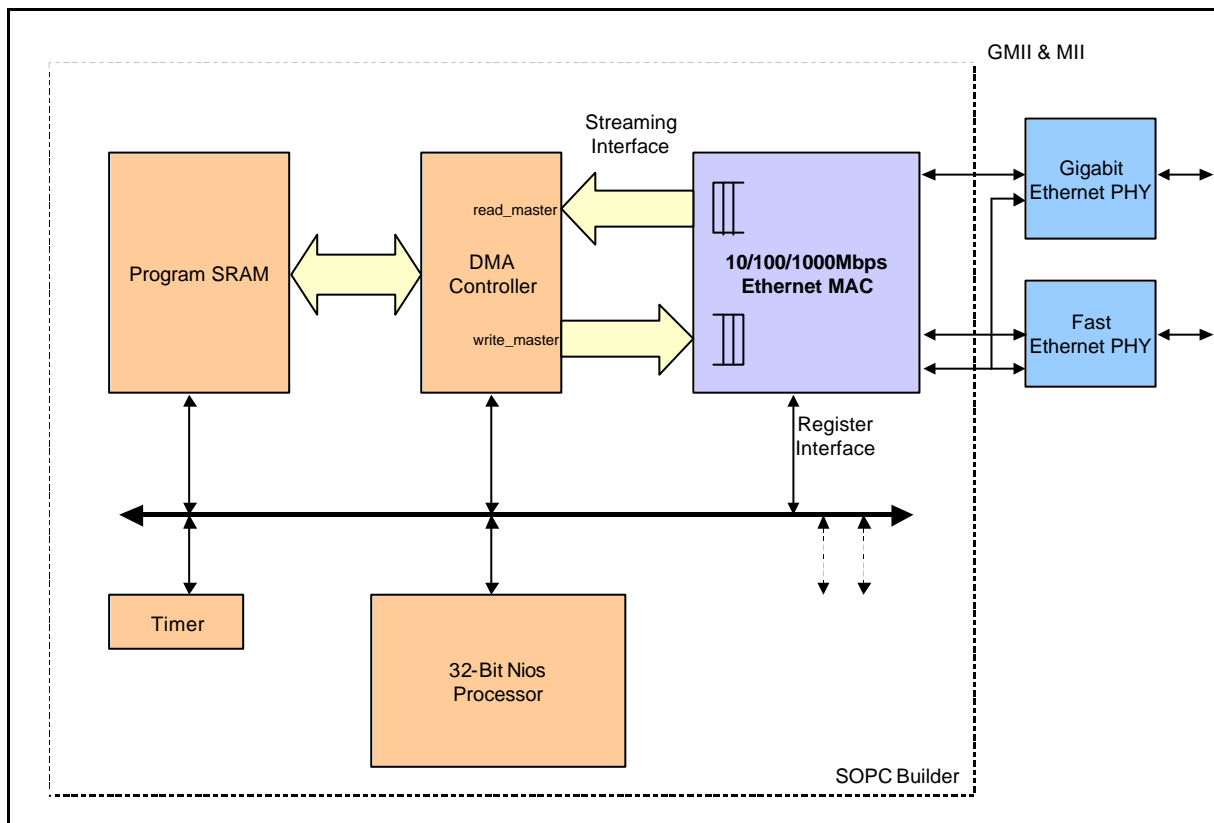


Figure 2: Application Example



## 3 10/100/1000 Mbps Ethernet MAC-NET Core Features

### 3.1 Ethernet MAC Feature Highlights

- Triple Speed 10/100/1000Mbps Ethernet MAC
- Preamble and SFD (Start of Frame delimiter) insertion and deletion
- Optional Padding termination/insertion for NIC applications or forwarding of unmodified frames for switching applications
- Supports AMD Magic Packet detection with interrupt for node remote power management
- Support for VLAN tagged frames according to IEEE 802.1Q specification in both transmit and receive
- CRC-32 checking at full speed using a multi-stage CRC calculation architecture with optional forwarding of the FCS field to the user application
- CRC-32 generation and append on transmit or forwarding of user application provided FCS selectable on a per-frame basis
- Individual, up to 5, Unicast MAC addresses for frame filtering or fully transparent operation
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16K Bytes
- Embedded programmable Multicast address resolution hash table
- Optional and programmable internal GMII / MII Loopback
- Programmable Half Duplex (10/100) or Full Duplex (10/100/1000) network operation
- Half Duplex collision and automatic frame re-transmission with Jamming and Back-Off timer
- In Full Duplex, optional automatic Pause Frame generation from programmable FIFO congestion thresholds or by dedicated command pin with programmable Quanta
- Programmable Automatic Xon and Xoff flow control frame generations
- Complete Network statistics with RMON and MIB/MIB-II Counters
- MDIO Master interface for PHY device configuration and management with two programmable MDIO base addresses
- 32-bit Avalon System Interface with separate slave ports for data and control
- Avalon data path ports with full streaming support allowing efficient DMA transactions
- Fully integrated in Altera SOPC Builder for ease of use and instant system generation

### 3.2 IP Protocol Performance Optimization Features

- Operates on TCP/IP and UDP/IP and ICMP/IP protocol data or IP header only
- Enables wire-speed processing up to Gigabit Ethernet
- Transparent passing of frames of other types and protocols
- Support for VLAN tagged frames according to IEEE 802.1q with transparent forwarding of VLAN tag and control field
- Automatic IP-header and payload (protocol specific) checksum calculation and verification on receive



# 10/100/1000Mbps Ethernet MAC with Protocol Acceleration MAC-NET Core with Avalon Interface

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## Product Brief

Version 1.0 - February 2004

- Automatic IP-header and payload (protocol specific) checksum generation and automatic insertion on transmit configurable on a per-frame basis
- Support for IP and TCP, UDP, ICMP data for checksum generation and checking
- Full header options support for IPv4 and TCP protocol headers
- IPv6 support limited to datagrams with base header only. Datagrams with extension headers are passed transparently unmodified/unchecked.
- Statistics information for received IP and protocol errors
- Configurable automatic discard of erroneous frames
- Configurable automatic Host-to-Network (RX) and Network-to-Host (TX) byte order conversion for IP and TCP/UDP/ICMP headers within the frame
- Configurable padding remove for short IP datagrams on receive
- Configurable Ethernet IPv4 and IPv6 Type removal on receive and automatic insertion on transmit to allow for 32-bit word aligned header and payload processing
- Store&Forward operation with clock and rate decoupling FIFOs
- Generic C software drivers and example programs
- Optimized TCP/IP stack reference implementation for use with embedded processor environments

4 MAC-NET Core Block Diagram

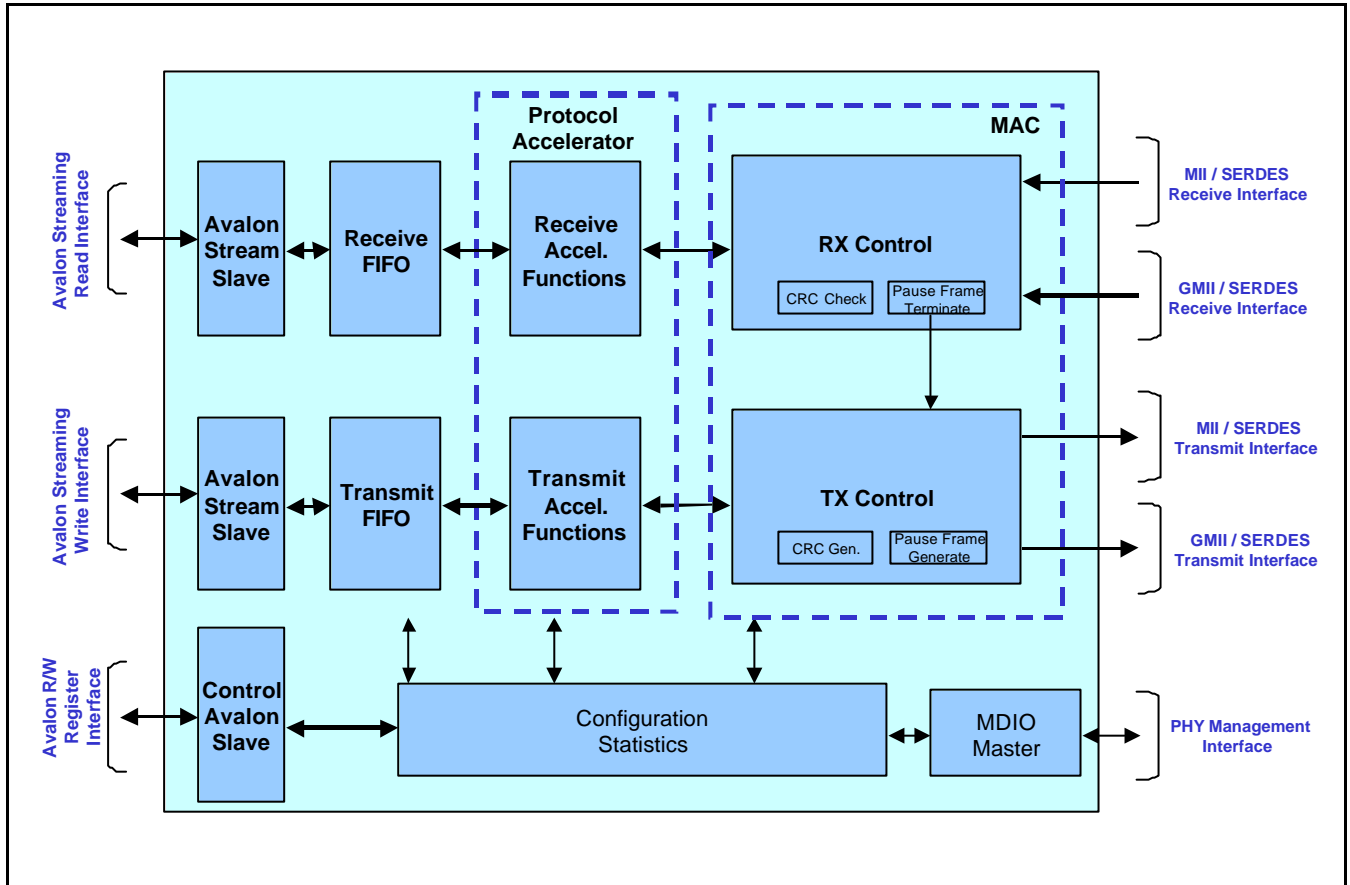


Figure 3: 10/100/1000Mbps Ethernet MAC with Accelerator Core Overview



## **5 Implementation Summary**

### **5.1 MAC-NET Core with Avalon Bus Interface**

**Table 1: 10/100/1000 Ethernet MAC-NET Complexity Summary**

<b>Target Device Family</b>	<b>Speed Grade</b>	<b>Complexity</b> (With 2048 Byte FIFO per direction)		<b>Performance</b>	<b>MAC Requirement</b> (Ethernet Speed)
		LEs	RAM bits		
STRATIX	-7	5080	45280	137 MHz	125MHz (Gigabit)
CYCLONE	-7	5090	45280	135 MHz	125MHz (Gigabit)



## **6 10/100/1000Mbps Ethernet MAC-NET Design Kit Overview**

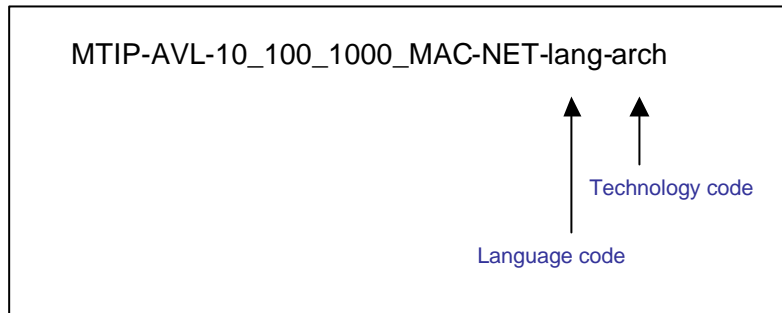
**Table 2: Design Kit Overview**

<b><i>Design and Simulation</i></b>	
Language	Optimized VHDL / Verilog or lower cost CPLD encrypted netlist.
Simulation	Configurable VHDL / Verilog Testbench with embedded frame generator and checker providing an easy to use and robust de-bugging environment.
Verification	Comprehensive test environment with Ethernet frame generator and verification models for standard compliant and errored frame generation and automated core behavior verification.
<b><i>Supported Design Tools</i></b>	
Simulation	Modelsim Version 5.7 or higher.
Synthesis	Exemplar 2002d or higher.
Implementation	Quartus II V3.0 or Higher, SOPC Builder 3.0 or higher

## **7 References**

1. IEEE 802.3 2002 Edition
2. IEEE 802.1Q 1998 Edition
3. RFC2665, Definitions of Managed Objects for the Ethernet-like Interface Type
4. RFC2863, The interfaces Group MIB
5. IETF RFC 791, Internet Protocol (IPv4)
6. IETF RFC 792, Internet Control Message Protocol (ICMP)
7. IETF RFC 793, Transmission Control Protocol (TCP)
8. IETF RFC 768, User Datagram Protocol (UDP)
9. IETF RFC 894, Transmission of IP Datagrams over Ethernet Networks
10. IETF RFC 2460, Internet Protocol, Version 6 (IPv6)
11. IETF RFC 2464, Transmission of IPv6 Packets over Ethernet Networks

## 8 Ordering Code

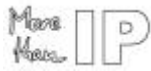


**Table 3: Language Code**

Technology Code	Target Technology
BIN	Encrypted CPLD netlist.
VHDL	Synthesizable generic VHDL source code for CPLD or ASIC implementations
VLOG	Synthesizable generic Verilog source code for CPLD or ASIC implementations

**Table 4: Technology Code**

Technology Code	Target Technology
GEN	Source code option for Altera CPLDs (APEX20KE, CYCLONE, APEX-II, STRATIX or STRATIX GX) or ASIC implementations.
ALTR	Encrypted netlist for Altera CPLDs (APEX20KE, APEX-II, CYCLONE, STRATIX or STRATIX GX).



## **9 Contact**

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