

1 Introduction

The Fibre Channel (FC) is logically a bi-directional point-to-point serial data channel, structured for high performance information transport. Physically, Fibre Channel is an interconnection of one or more point-to-point links. Each link end terminates in a Port. Ports are fully specified in the Physical Interface (FC-PI) specification and Framing and Signaling (FC-FS) specification. Fibre is a general term used to cover all physical media supported by Fibre Channel including optical fiber, twisted pair, and coaxial cable.

Serial data streams are supported at data rates of 1,06 Gbaud, 2,12 Gbaud, 4,25 Gbaud and 10,2 Gbaud. All data rates have transmitter and receiver clock tolerances of ± 100 ppm.

Fibre Channel is structured as a set of hierarchical functions as illustrated in Figure 1. Fibre Channel consists of related functions FC-0 through FC-3. Each of these functions is described as a level. Fibre Channel does not restrict implementations to specific interfaces between these levels.

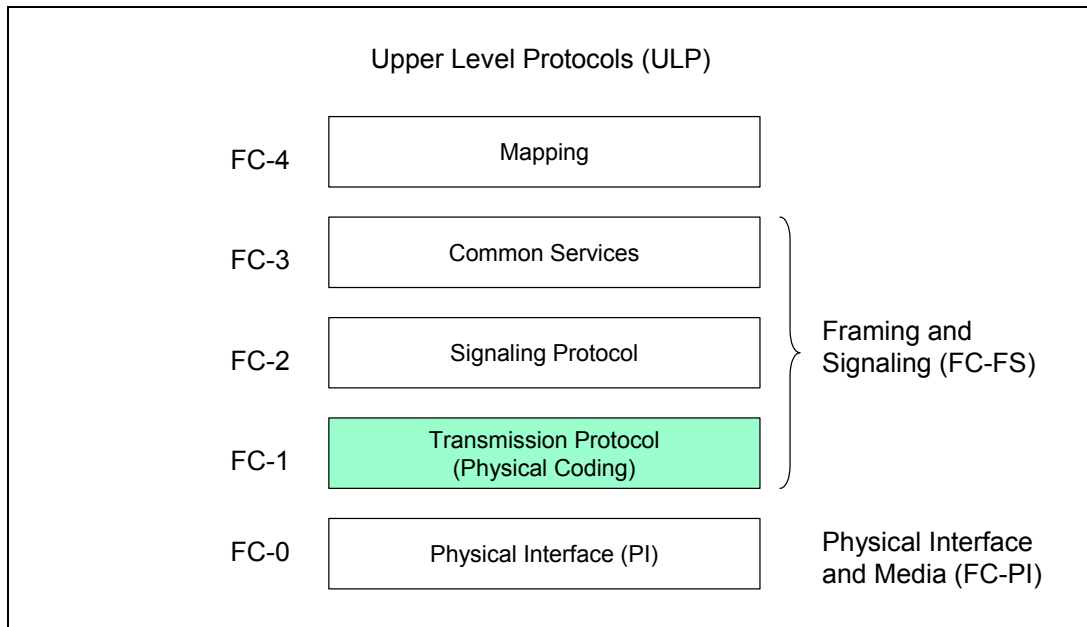


Figure 1: Fibre Channel Function Hierarchy

The 10 Gigabit Fibre Channel FC-1 Core performs the FC-1 layer functions and is designed to comply with the T11 10GFC Rev 3.0 draft specification.

The FC-1 level generates continuous data or control characters on the transmit path and expects continuous data or control characters on the receive path. The FC-1 level participates in link fault detection and reporting by monitoring the receive path for status reports that indicate an unreliable link, and generating status reports on the transmit path to report detected link faults to the FC-1 level on the remote end of the link. 10GFC provides the specification of optional physical interfaces applicable to the implementation of 10GFC Ports. In addition, the 10GFC FC-1 level specifies optional electrical interfaces which may be used to interconnect the physical embodiment of various sublayers. These interfaces include the 10 Gigabit Media Independent Interface (XGMII) and the 10 Gigabit Attachment Unit Interface (XAUI). One or both of these interfaces may typically be present within a 10GFC port.

The 10 Gigabit FC-1 Core is available for Altera CPLD or ASIC implementations.

2 10G FC-1 Core Description

The 10G FC-1 core includes line scrambler/descrambler, the 64b/66b encoder/decoder, block synchronization and gearbox as well as clock and rate decoupling elastic buffers (FIFO).

On the application side, the Core can be configured to implement either a XGMII (10 Gigabit Medium Independent Interface) or a XAUI (10 Gigabit Attachment Unit Interface) when the design is targeted to Altera Stratix GX CPLD. Typically, the XGMII interface is selected when the Core is integrated, together with custom logic, in a CPLD or an ASIC solution while the XAUI interface provides a simpler 16-Bit board level interface to connect the Core to a FC-2 layer device.

On the line side, the MorethanIP 10G FC-1 Core, implements a 64-Bit interface which is typically connected, via a SFI Mux / Demux, to a XSBI interface operating at 644.53 MHz. The SFI Mux / Demux is, as an example, implemented with Stratix high speed LVDS I/O Macros.

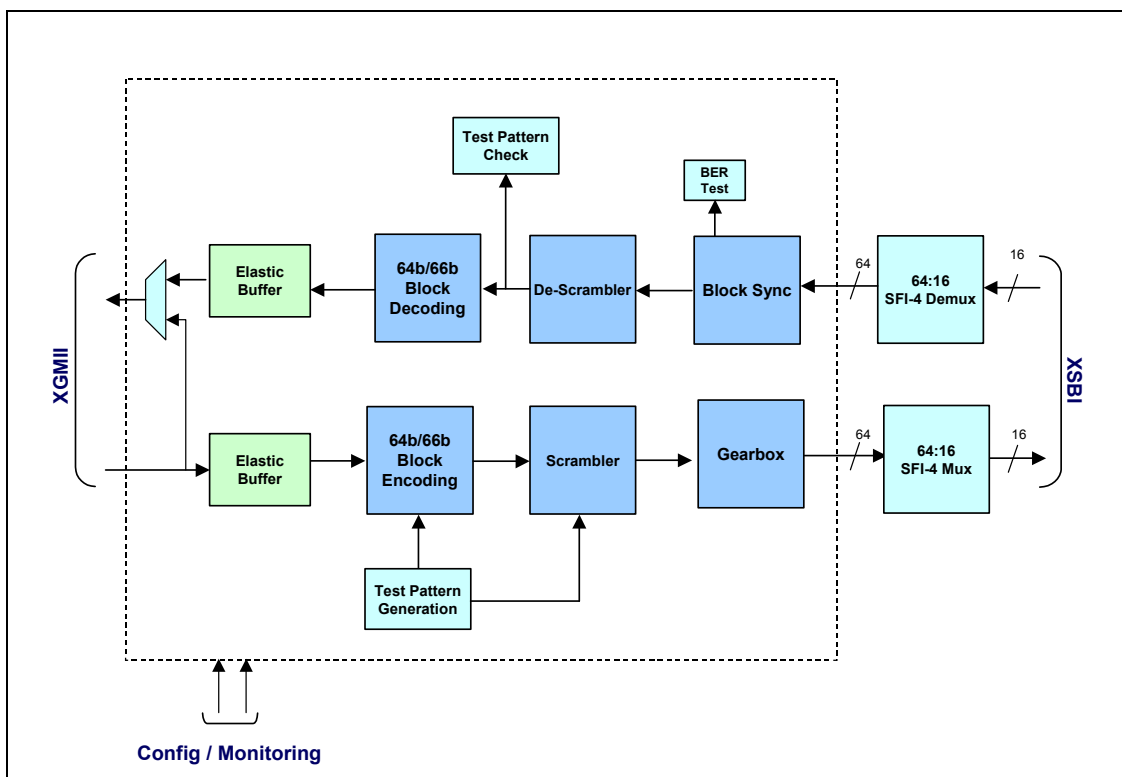


Figure 2: 10G FC-1 Block Diagram

3 10G FC-1Core Features

- Compliant with the T11 10GFC Rev 3.0 and IEEE802.3ae specification
- Optional Media independent 64-Bit non-DDR Interface or standard 32-bit XGMII DDR interface to connect to FC-2 and higher layers
- Optional XAUI interface implemented with embedded Quad SERDES providing an efficient board level interface to optical modules and loopback
- Optional XAUI interface compatible with Xenpak V2.0 specification
- Implements 4:1 XSBI Mux / Demux when selected technology is Altera CPLD to connect to FC-0 physical layers
- Implements 10GFC data Scrambler which generates a transition rich signals to the application high speed optical link and data De-Scrambler on the Core receive path
- 64/66b data coder / decoder with synchronization header insertion / deletion on transmit / receive respectively
- 66b block synchronization on the receive path and 66b block encoding on transmit with gearbox function
- 64b/66b Encoder/Decoder performing 66-bit word alignment, the 64b/66b receive path decoding, the 64b/66b transmit path encoding, and the 66b/64b transmit path conversion for block overhead bits.
- Implements XGMII / XSBI clock rate decoupling with elastic buffers on the transmit and receive paths
- Rate Matching FIFO with idle insertion/removal in receive direction simplifying system clock distribution
- Programmable loopback on the Core XGMII interface available for application test
- Implements Test Pattern Generator/Checker for link testing and in-system testing
- Implement Bit Error Rate (BER) monitoring, with high error rate indication, providing constant line quality monitoring
- Available for Altera Stratix CPLDs (Complex Programmable Logic Devices) or for ASIC implementation which provides time to market and cost effective solutions
- Complete design kit which includes Frame generators and checking models, standard compliance scenario and implementation scripts for various ASIC and Programmable Logic technologies

4 Implementation Summary

Table 1: Altera STRATIX Implementation Summary

<i>Device</i>	<i>Complexity</i>		<i>Max. Freq.</i>
	<i>Logic Elements</i>	<i>Memory Bits</i>	
STRATIX (EP1S25)	6300 (23% Utilization)	7K (<1% Utilization)	>161.13MHz (-C6)

5 Design Package and Support

- Delivered, optionally, as an Altera CPLD netlist or in Register Transfer Level (RTL) synthesizable VHDL / Verilog source code
- Configurable VHDL / Verilog verification test-benches for automated design testing
- Scripts for Exemplar Leonardo Spectrum synthesis tools
- Script for Altera Quartus-II implementation software
- Detailed user's and methodology guides

6 Ordering Information

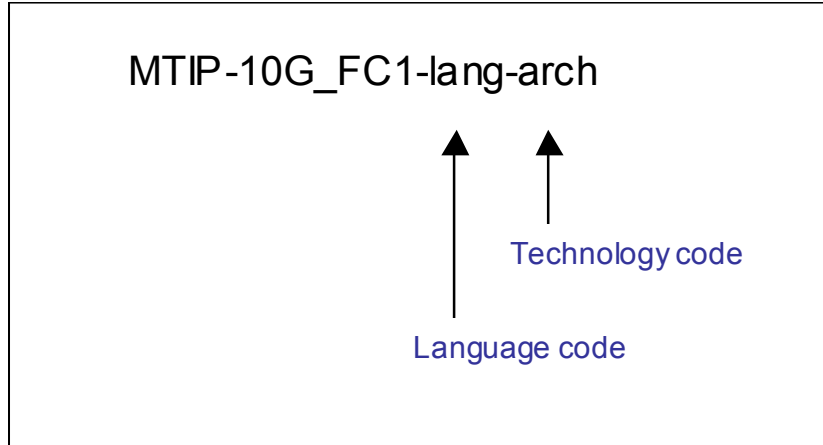


Table 2: Language Code

<i>Language Code</i>	<i>Delivery Language</i>
VHDL	Synthesizable RTL VHDL
VLOG	Synthesizable RTL Verilog
BIN	Encrypted netlist for Altera CPLD or ASSP devices

Table 3: Technology Code

<i>Technology Code</i>	<i>Target Technology</i>
GEN	Fully generic sythesizable code for ASIC or Altera Stratix / Stratix GX CPLD
ALTR	Netlist for Altera Stratix, Stratix GX CPLDs

7 Contact

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