

1 Introduction

Initially, network managers use 10 Gigabit Ethernet to provide high-speed, local backbone interconnection between large-capacity switches. 10 Gigabit Ethernet enables Internet Service Providers (ISPs) and Network Service Providers (NSPs) to create very high-speed links at a very low cost, between co-located, carrier-class switches and routers. The technology also allows the construction of MANs and WANs that connect geographically dispersed LANs between campuses or points of presence (PoPs). These connections use dark fiber, dark wavelengths, or SONET (synchronous optical network) networks. 10 Gigabit Ethernet provides, for MAN and WAN, compatibility with the installed OC-192 SONET rings.

As the demand for bandwidth increases, 10 Gigabit Ethernet will be deployed throughout the entire network, and will include server farms, backbones, and campus-wide connectivity.

Ethernet provides significant advantages over other technologies, such as ATM. 10 Gigabit Ethernet extends the capabilities, to WAN and MAN connectivity, of lower rates (10/100 and Gigabit) Ethernet links to build end to end Ethernet networks with proven, simple and low cost solutions:

- No expensive, bandwidth-consuming conversion between Ethernet frames and ATM cells is required; the network is Ethernet, end to end.
- The combination of IP and Ethernet offers Quality of Service and traffic policing capabilities that approach those provided by ATM, so that advanced traffic engineering technologies are available to users and providers.
- A wide variety of standard optical interfaces (wavelengths and link distances) have been specified for 10 Gigabit Ethernet, optimizing its operation and cost for LAN, MAN, or WAN applications.

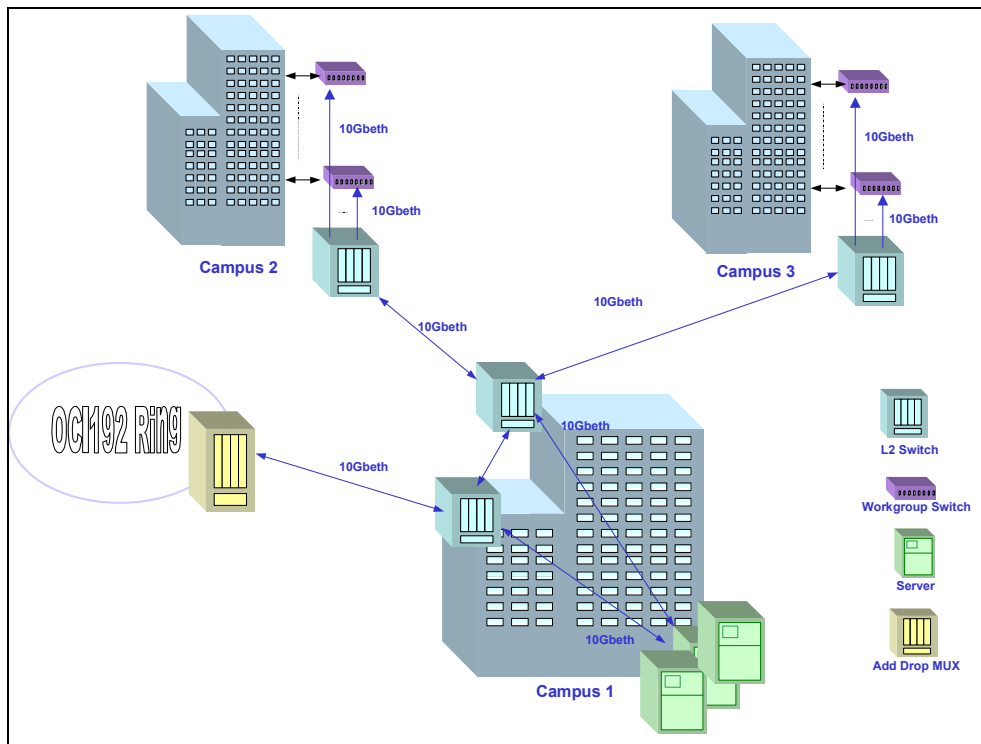


Figure 1: 10 Gigabit Ethernet Deployment Example

Product Brief
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The 10 Gigabit Ethernet MAC core is designed to comply with the IEEE 802.3ae Draft 3.2 specification and to meet the requirements for both WAN/MAN and LAN applications. The MAC layer also implements automatic flow-control and support for virtual bridged LANs (VLAN, IEEE 802.1Q specification).

The 10 Gigabit Ethernet MAC core implements, on the application side, a flexible FIFO interface designed to be seamlessly connected to any MorethanIP standard Telecom Interface (e.g. SPI-4 or POS-PHY L4). On the Ethernet Line side, the MAC core implements an interface designed to be connected to vendor specific XGMII DDR (Dual Data Rate) I/O structure.

An optional host interface is available to connect the Ethernet MAC core to a configuration and management host processor.

The following figure shows an application example with a 10 Gigabit Ethernet line card with a LAN PHY physical layer.

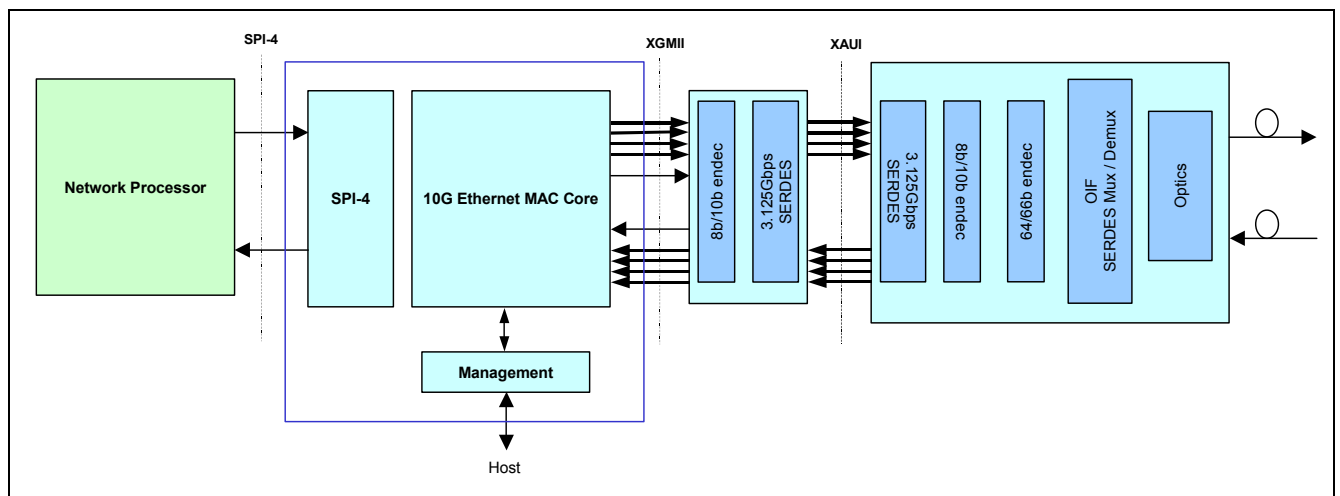


Figure 2: 10 Gigabit Ethernet MAC Core Application Example

2 10 Gigabit Ethernet MAC Core Features Overview

- Full MAC and Reconciliation layer and sub-layer implementation compliant with IEEE802.3ae draft 3.3 specification
- Direct interface to standard 32-Bit DDR (Dual Data Rate) XGMII connections or to a selection of high speed SERDES devices via 32-Bit SSTL-II, HSTL Class I
- Lane, data alignment and PHY error handled by the core reconciliation sub-layer
- CRC-32 generation and checking at full speed using a multi-stage CRC calculation architecture
- Unicast, Broadcast and Multicast Ethernet Frames supported in both transmit and receive
- Dynamically programmable MAC address with promiscuous mode option
- Multicast address filtering with 64-bin hash code lookup table on receive reducing processing load on higher layers
- Automatic discard of errored received frames, for example frames with preamble, length or type error
- Ethernet Pause Frame (802.3 Annex 31A) and termination providing fully automated flow control without any user application overhead
- Automatic Pause Frame generation from programmable FIFO congestion thresholds and programmable Quanta
- Pause frame generation optionally controlled by a command pin offering flexible application traffic flow control
- Programmable frame maximum length providing support for any frame (e.g. Jumbo Frame or any tagged Frame)
- Support for VLAN tagged frames according to IEEE 802.1Q specification in both transmit and receive
- Dynamic inter packet gap (IPG) calculation for WAN applications
- Simple 64 bit interface to user application with seamless interconnection to other MorethanIP telecom interface cores (e.g. SPI-4)
- Fully programmable FIFOs providing rate and clock decoupling on the interface to the user application
- In-System programmable FIFO threshold settings for system level performance optimization
- Status word available with each Frame on the User interface providing information such as frame length, Frame type indication, VLAN tag and error information
- Frame padding, preamble and SFD (Start of Frame Delimiter) / insertion and deletion
- User interface supports data rates up to 12.5Gbps with full back to back Frame transfer support
- Implements statistics and event signals to providing support for 802.3 basic and mandatory Management Information Database (MIB) package (RFC2665) required in SNMP environments
- Design Kit includes with Ethernet frame generators and checking models enabling fully automated design verification, standard compliance test, providing fast turn-around design cycles and regression testing

3 10 Gigabit Ethernet MAC Core Block Diagram

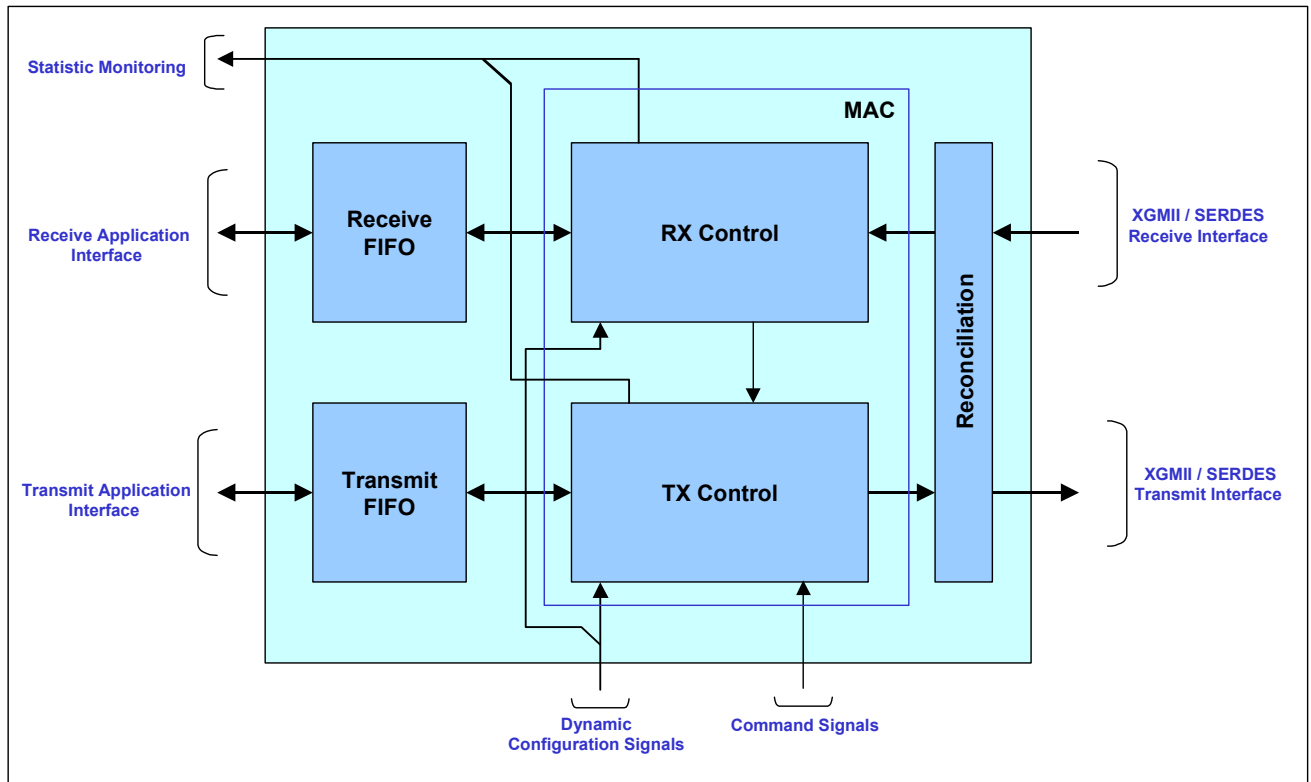


Figure 3: 10 Gigabit Ethernet MAC Core Block Diagram

4 Implementation Summary

Table 1: Altera APEX II Implementation Summary

Device	FIFO Sizes	Size (LCells)	Freq.
EP2A15	TX: 256x64 RX: 256x64	7500 (45% Utilization)	>156.25 MHz (C7)
EP2A25	TX: 256x64 RX: 256x64	7500 (28% Utilization)	>156.25 MHz (C7)
EP2A70	TX: 256x64 RX: 256x64	7500 (10% Utilization)	>156.25MHz (C7)

Table 2: Altera STRATIX Implementation Summary

<i>Device</i>	<i>FIFO Sizes</i>	<i>Size (LCells)</i>	<i>Freq.</i>
EP1S10	TX: 512x64 RX: 512x64	7340 (69% Utilization)	>156.25 MHz (C7)
EP1S20	TX: 512x64 RX: 512x64	7340 (39% Utilization)	>156.25 MHz (C7)
EP1S40	TX: 512x64 RX: 512x64	7340 (17% Utilization)	>156.25 MHz (C7)
EP1S80	TX: 512x64 RX: 512x64	7340 (9% Utilization)	>156.25MHz (C7)

5 Design Package and Support

- Delivered, optionally, as an Altera CPLD netlist or in fully generic Register Transfer Level (RTL) synthesizable VHDL or Verilog source code
- Configurable VHDL verification test-benches with complete Ethernet Frame generator and Ethernet Frame monitor for fully automated design testing. Dedicated compliance test suite for regression testing
- Scripts for synthesis tools and Altera Quartus-II architecture layout tool
- Detailed user's and methodology guides

6 Ordering Information

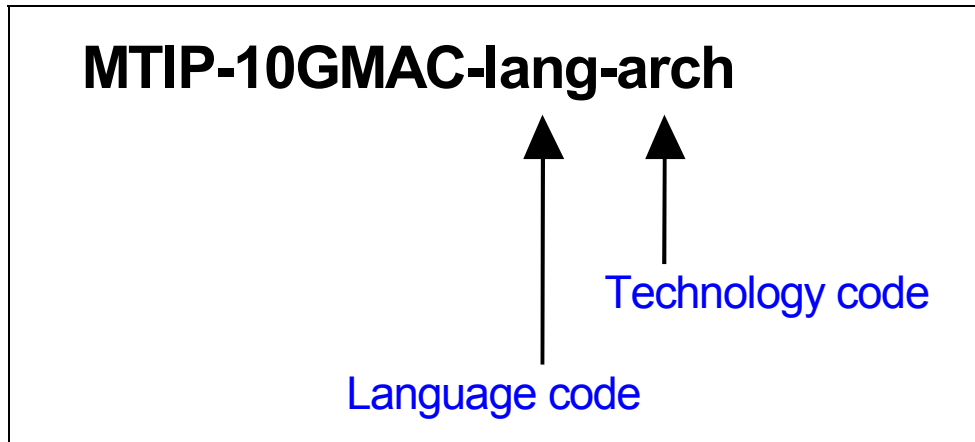


Table 3: Language Code

<i>Language Code</i>	<i>Delivery Language</i>
VHDL	Synthesizable RTL VHDL
VLOG	Synthesizable RTL Verilog
BIN	Encryped CPLD netlist

Table 4: Technology Code

<i>Technology Code</i>	<i>Target Technology</i>
GEN	Fully generic sythesizable code for ASIC or Altera CPLD implementations
APX	Netlist for Altera APEX-II CPLD
STX	Netlist for Altera STRATIX CPLD

7 Contact

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