

1 Introduction

The Fibre Channel (FC) is logically a bi-directional point-to-point serial data channel, structured for high performance information transport. Physically, Fibre Channel is an interconnection of one or more point-to-point links. Each link end terminates in a Port. Ports are fully specified in the Physical Interface (FC-PI) specification and Framing and Signaling (FC-FS) specification. Fibre is a general term used to cover all physical media supported by Fibre Channel including optical fiber, twisted pair, and coaxial cable.

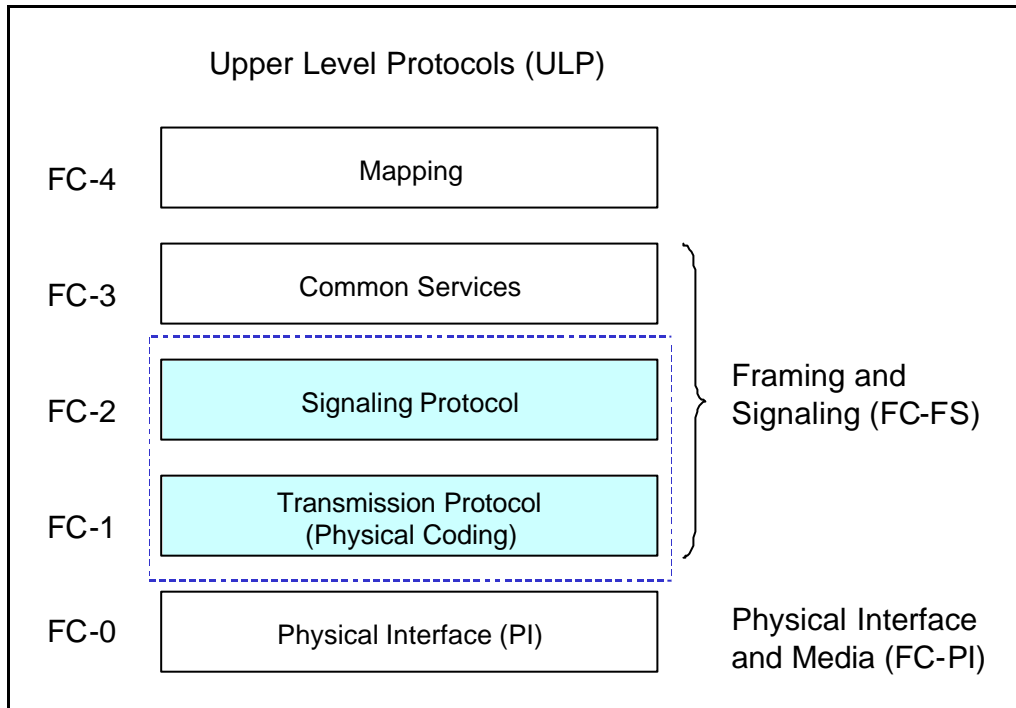


Figure 1: Fibre Channel Function Hierarchy

The Gigabit / 2-Gigabit FC-2 Core provide a generic solution for 1Gbps and 2Gbps Fibre Channel applications. The core is designed to support standard Fibre Channel applications such as point-to-point as well as fabric interconnect. On the Client side, the Core implements a 16-Bit FIFO interface running asynchronously from the Fibre Channel line clock. The FC-2 Layer provides services such as CRC generation / check, generate Fibre Compliant frames and buffer-to-buffer credit with necessary Fibre Channel timers and link set-up FC_PORT state machine.

The FC-1 function implements the line coding (8B/10B), maintains DC balancing on the line, performs frame encapsulation, Fibre Channel Primitive Sequences generation / decoding, receive data alignment and link synchronization. On the line interface, the Core implements a standard 10-Bit or 20-Bit interface that can be connected to any commercial or embedded (With Altera StratixGX devices) SERDES (SERializer / DESerializer).

The Core can be targeted to programmable devices, for system prototyping and validation and ASIC technologies.

2 Multi-Gigabit Fibre Channel Transport Core Features

- Dynamically configurable to support Gigabit (1.06Gbps Baud rate) or 2 Gigabit (2.12Gbps Baud rate) Fibre Channel applications
- Fibre Channel logic operates at rates up to 106.25MHz
- Seamless interface to commercial SERDES device or Fibre Channel control via a standard 10-Bit (Gigabit Operation) or 20-Bit (Two Gigabit Operation) interface
- Built-In client interface FIFO providing rate and clock decoupling
- Simple 16-Bit FIFO interface to user client application compatible with Altera Atlantic specification
- CRC-32 checking at 106.25MHz wire speed using a multi-stage CRC calculation architecture
- Optional CRC check and correction on the Core transmit path controllable on a frame by frame basis
- Frame minimum and maximum length verification with long frame truncation and error indication
- Link coding implemented with 8B/10B providing DC balanced bitstream for efficient SERDES operation
- Maintain 8B/10B current disparity rules with automatic correction using positive or negative encoded EOF primitives
- Negative encoded K28.5 Comma detection with automatic optical stream alignment
- Implements FC-1 link synchronization with Loss of Synchronization indication
- Implements Fibre Channel FC_PORT Port control state machine with programmable timers
- Core configurable as N or F Fibre Channel port with automatic Fabric frames discard (N Port configuration)
- Provide FC Transport support for point-to-point Fibre Channel applications
- Support any Fibre Channel Traffic Class and Frame termination condition
- Implement Buffer-to-Buffer Credit management with credit recovery, credit reset and automatic R_RDY, BB_SCr and BB_SCs primitives generation
- Programmable 16-Bit credit recovery timer
- Programmable Transmit and Receive FIFO depth
- Implements processor control interface with 32-Bit statistic counters and configuration registers
- Simple handshake user application FIFO interface with fully programmable depth and threshold levels ensuring data rates of 2Gbps with full back-to-back frame transfer support
- Available on Altera StratixGX devices with integrated SERDES providing a single chip Fibre Channel port controller implementation

3 Block Diagram

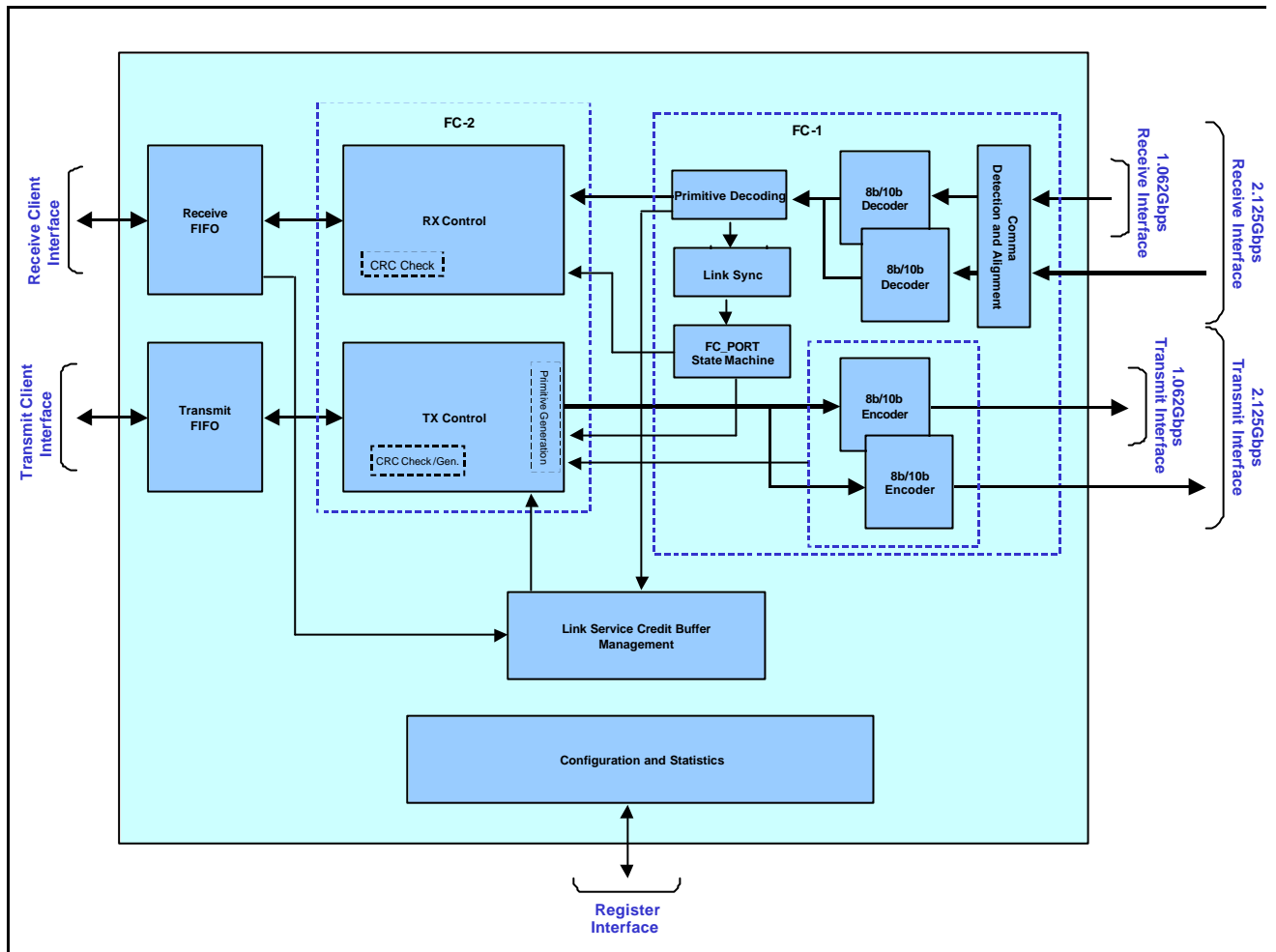


Figure 2: Multi-Gigabit Fibre Channel Transport Core Overview

4 Implementation Summary

Table 1: Multi-Gigabit Fibre Channel Transport Complexity Summary

Target Device Family	Speed Grade	Complexity With 3 Receive Buffer 256-Byte Transmit FIFO	Performance	Requirement
		LEs		
STRATIX (EP1S10)	-7	4000	115MHz	106.25MHz
STRATIX-GX (EP1S10)	-7	4000	115MHz	
CYCLONE (EP1C4)	-7	4000	118MHz	

5 Deliverables Overview

Table 2: Deliverables Overview

<i>Design and Simulation</i>	
Language	Optimized VHDL or Verilog or lower cost encrypted netlist for Altera FPGA devices.
Simulation	Configurable VHDL or Verilog Testbench with embedded frame generator and checker providing an easy to use and robust de-bugging environment.
Verification	Comprehensive RTL and Gate Level verification environments with Fibre Channel frame generator and verification models for standard compliant and errored frame generation and automated core behavior verification.
Synthesis	Scripts for industry standard ASIC and FPGA Synthesis tools.
Implementation	Quartus-II Script file.

6 Ordering Code

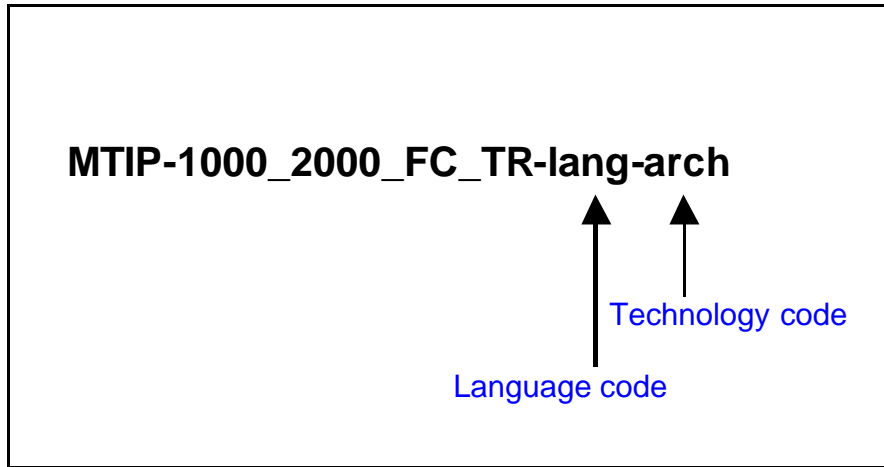


Table 3: Language Code

<i>Technology Code</i>	<i>Target Technology</i>
BIN	Encrypted CPLD netlist.
VHDL	Synthesizable generic VHDL source code for CPLD or ASIC implementations
VLOG	Synthesizable generic Verilog source code for CPLD or ASIC implementations

Table 4: Technology Code

<i>Technology Code</i>	<i>Target Technology</i>
GEN	Generic source code.
ALTR	Encrypted netlist for Altera CPLD.

7 Contact

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