

Q. What power analysis tools are available from Altera?

A. Altera's PowerPlay power analysis technology features Excel-based PowerPlay early power estimators and Quartus® II PowerPlay power analyzer tools. You can download PowerPlay early power estimators from Altera's website for the specific device family. PowerPlay power analyzer is embedded with Quartus II software. These power analysis tools give you the ability to estimate power consumption from early design concept through design implementation.

Q. When should I use the PowerPlay early power estimator tool?

A. Use the PowerPlay early power estimator to estimate your design's power usage before creating the design or during the design process. You can perform preliminary thermal analysis of your design and plan for power management.

Q. When should I use the PowerPlay power analyzer tool?

A. Use the PowerPlay Power Analyzer Tool to obtain an accurate estimation of power after the design is complete, ensuring that thermal and supply budgets are not violated.

Q. What are the inputs to the Quartus II PowerPlay Power Analyzer?

A. The power analyzer provides a flexible framework for specifying signal activities. This reflects the importance of using representative signal activity data during power analysis. Use the following sources to provide information about signal activity:

- Simulation results
- User-entered node, entity, and clock assignments
- User-entered default toggle rate assignment
- Vectorless estimation

The PowerPlay power analyzer also lets you mix and match the signal activity data sources on a signal-by-signal basis.

Q. How accurate are the power analysis results?

A. The accuracy of power estimation depends on the stage of the design. For a partially completed design or in the concept phase, use the PowerPlay early power estimator to obtain an initial power estimate. For designs that are completed, simulation-based power estimation generated from the PowerPlay power analyzer provides an accurate power estimation compared to early power estimates.

Altera's Quartus II PowerPlay power analyzer tool is accurate (to within 20%) of actual device power consumption, provided that supplied input vectors are representative of typical design operation. The accuracy of the results of the early power estimator is generally within $\pm 20\%$ of the Quartus II PowerPlay power analyzer estimates, assuming perfect toggle-rate entry.

Q. Is the simulation-based power analyzer in Quartus II software more accurate than the early power estimator?

A. Yes. The simulation-based power analyzer in Quartus II software is more accurate because it uses design details such as routing, placement, and simulation results to improve the accuracy.

Q. How do I generate a simulation results file (SAF or VCD) to use with the Quartus II power analyzer tool?

A. Signal activity and static probability information are stored in a Signal Activity File (.saf) generated by the Quartus II simulator or may be derived from a Value Change Dump File (.vcd) generated by the Quartus II simulator or EDA simulators.

Refer to the [PowerPlay Power Analysis \(PDF\)](#) chapter of the *Quartus II Development Software Handbook* for information on how to generate .saf and .vcd files.

Q. How do I optimize the design for power in Quartus II software?

A. Quartus II software offers power-driven compilation to fully optimize device power consumption. Power-driven compilation focuses on reducing your design's total power consumption using power-driven synthesis and power-driven place-and-route.

For additional information on different power optimization techniques, refer to the [Power Optimization \(PDF\)](#) chapter of the *Quartus II Development Software Handbook*.

Q. What is Programmable Power Technology?

A. Programmable Power Technology allows you to program the core logic in Stratix® III and Stratix IV FPGAs for high speed or low power, depending on design requirements. Programmable Power Technology enables Stratix III and Stratix IV FPGAs to deliver the lowest power and the highest performance.

For example, to set an NMOS transistor in the core of Stratix IV FPGAs to:

- Low-power mode, Quartus II software reduces the back bias voltage (making it more negative), which makes the transistor harder to turn on. This reduces the leakage current and saves power.
- High-performance mode, Quartus II software increases the back bias voltage (making it less negative), which makes the transistor easier to turn on in the few timing-critical paths to help meet the design's specified timing constraints and deliver the maximum performance.

Quartus II software automatically controls which logic operates in high-speed mode and which operates in low-power mode, based on the timing constraints specified for the design.

For additional information on Programmable Power Technology, refer to the [40-nm Power Management and Advantages \(PDF\)](#) white paper.