



In-System Programmability in MAX Devices

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Application Note 95

Introduction

MAX® devices are programmable logic devices (PLDs), based on the Altera® Multiple Array MatriX (MAX) architecture that supports the IEEE Std. 1149.1 Joint Test Action Group (JTAG) interface. MAX devices are also in-system programmable, which adds programming flexibility and provides benefits in many phases of product development, manufacturing, and field use. This application note provides background information on in-system programmability (ISP) and the IEEE Std. 1149.1 JTAG interface and discusses the advantages of using ISP-capable MAX devices.

Features & Benefits

In-system design, prototyping, and manufacturing, reduces cost, shortens development time, and provides a wider range of programming options than standard device programming methods. With ISP, you can:

- Program and reprogram devices after they are soldered onto the printed circuit board (PCB), minimizing the possibility of lead damage or electrostatic discharge (ESD) exposure.
- Manufacture systems before you finalize device configuration.
- Perform boundary-scan test (BST) procedures and program devices using in-circuit testers.
- Upgrade systems in the field after they have been shipped.

Table 1 describes the features and benefits of using ISP-capable MAX devices.

| Table 1. ISP-Capable MAX Device Features & Benefits | | |
|----------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Development Phase | Features | Benefits |
| Device prototyping | Devices are programmed with a V_{CC} -level programming voltage. | Eliminates the need for a 12.0-V programming voltage and the possibility of accidental damage to lower voltage parts. Also reduces system power requirements. |
| | Devices can be programmed while soldered to a PCB. | Minimizes device handling, thereby protecting devices from ESD and lead damage. |
| | Prototype systems can be assembled before the device configuration is finalized. | Cuts prototype development time and saves development costs. |
| System manufacturing | PLDs can be treated the same way as other board-level devices because they can be programmed after the PCB is assembled. | Simplifies manufacturing, saves time, and protects devices from ESD and lead damage. |
| | ISP is implemented using the IEEE Std. 1149.1 (JTAG) interface; therefore, circuit testing and device programming can be combined into a single manufacturing step using a standard in-circuit tester. | |
| | Programming data can be downloaded from in-circuit testers, PCs, or workstations during final PCB test. | |
| | Devices can be programmed with test configurations. | Enhances design debugging and board-level testing capabilities. |
| In-field programming | Devices can be reprogrammed in the field. | Adds versatility and reduces service costs, thereby making products more attractive to the consumer. |

V_{CC}-Level Programming

ISP-capable MAX devices support ISP through a V_{CC} -level programming voltage. The devices generate a 12.0-V programming voltage internally to program, verify, and erase the device’s EEPROM cells, eliminating the need for the external 12.0-V programming voltage typically required for programming.

ISP-capable MAX devices are guaranteed for 100 erase and programming cycles with 100% programming and functional yields.

Programming Systems

In Altera devices, ISP is implemented using the IEEE Std.1149.1 JTAG interface, which streamlines PCB testing and device programming operations into a single manufacturing step.

ISP-capable MAX devices are supported by the following systems:

- MAX+PLUS II development system
- In-circuit testers
- Embedded processors

MAX+PLUS II Development System

You can use a PC or UNIX workstation, the MAX+PLUS II Programmer, and the BitBlaster™ serial or ByteBlasterMV™ parallel port download cable to download Programmer Object Files (**.pof**), Jam Files (**.jam**), or Jam™ Byte-Code Files (**.jbc**) from the MAX+PLUS II software to ISP-capable MAX devices mounted on a PCB. This method is more cost-effective than other programming methods because design, simulation, and prototyping can be performed using the same PC- or UNIX workstation-based system.

For production, you can implement ISP using Altera's free stand-alone programming software and the BitBlasterMV cable to download POFs.


 PC-based stand-alone programming software, **asap2.exe**, is available from Altera's FTP site at **ftp.altera.com** in the **\pub\misc** directory.

Figure 1 shows the 10-pin female plug dimensions for the BitBlaster or ByteBlasterMV download cable.

Figure 1. 10-Pin Female Plug Dimensions

Dimensions are shown in inches. The spacing between pin centers is 0.1 inch.

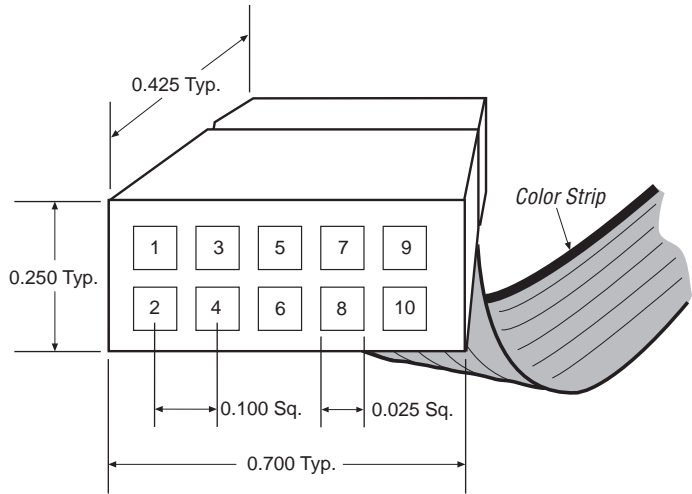


Table 2 identifies the 10-pin female plug's pin names for the corresponding download mode.

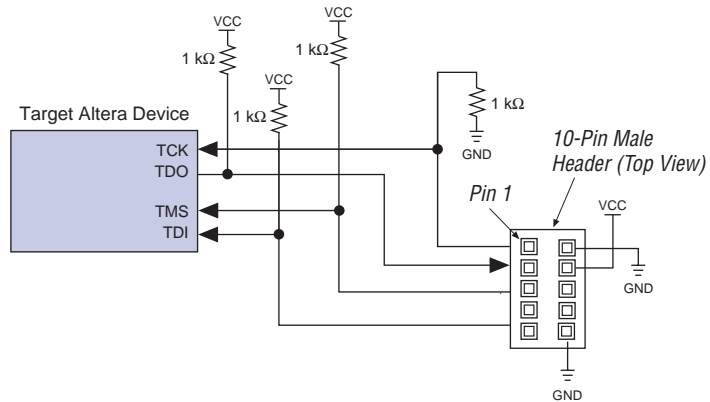
| Table 2. Female Plug's Pin Names & Download Modes | | | | |
|--------------------------------------------------------------|--------------------|----------------------------|--------------------|-----------------------|
| Pin | JTAG Mode | | PS Mode | |
| | Signal Name | Description | Signal Name | Description |
| 1 | TCK | Clock signal | DCLK | Clock signal |
| 2 | GND | Signal ground | GND | Signal ground |
| 3 | TDO | Data from device | CONFIG_DONE | Configuration control |
| 4 | VCC | Power supply | VCC | Power supply |
| 5 | TMS | JTAG state machine control | nCONFIG | Configuration control |
| 6 | – | No connect | – | No connect |
| 7 | – | No connect | nSTATUS | Configuration status |
| 8 | – | No connect | – | No connect |
| 9 | TDI | Data to device | DATA0 | Data to device |
| 10 | GND | Signal ground | GND | Signal ground |



The circuit board must supply V_{CC} and ground to the ByteBlasterMV cable.

ISP-capable devices are programmed via a device's JTAG pins: TCK, TMS, TDI, and TDO. Figure 2 shows how the BitBlaster or ByteBlasterMV download cable interfaces with an ISP-capable device. The I/O pins are tri-stated during in-system programming.

Figure 2. ISP-Capable MAX Device Programming with the BitBlaster or ByteBlasterMV Download Cable



Search for “Programming a Single Device with the BitBlaster or ByteBlasterMV” in MAX+PLUS II Help, or go to the *BitBlaster Serial Download Cable Data Sheet* and *ByteBlasterMV Parallel Port Download Cable Data Sheet* in this handbook for more information.

In-Circuit Test Programming

You can program ISP-capable MAX devices during the final PCB testing stage using in-circuit testers and the IEEE Std. 1149.1 (JTAG) interface. To program a device using in-circuit testers, create a Jam or SVF File with the MAX+PLUS II software and download this file from an in-circuit test station to one or more ISP-capable MAX devices.

Embedded Processor Programming

You can program ISP-capable MAX devices in-system using an embedded processor. For example, programming information can be stored in an EPROM and shifted into the ISP-capable MAX device using a 4-bit interface from the processor to the device's JTAG pins. This method lets you program devices during burn-in and upgrade devices in the field.

You can program MAX devices with an embedded processor by creating a Jam File from the MAX+PLUS II software and downloading it with the Jam Player.



Refer to *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor* for more information on embedded processor programming.

IEEE Std. 1149.1 Interface

MAX device JTAG pins and functions are described in [Table 3](#).

| Table 3. JTAG Pins | | |
|---------------------------|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Pin | Description | Function |
| TDI | Test data input | Serial input pin for data and instructions, which are shifted in on the rising edge of TCK. This signal needs to be externally pulled high during normal operation. |
| TDO | Test data output | Serial data output pin for instructions and data. Data is shifted out on the falling edge of TCK. This signal is tri-stated if data is not being shifted out of the device. |
| TMS | Test mode select | Input pin controls the IEEE Std. 1149.1 JTAG state machine and is evaluated on the rising edge of TCK. This signal needs to be externally pulled high during normal operation. |
| TCK | Test clock | Provides the clock signal for the JTAG circuits. The maximum operating frequency is 10 MHz. This signal needs to be externally pulled low during normal operation. |

During erasure, programming, and verification, all device I/O pins are tri-stated to eliminate interference from other devices on the PCB. Devices are programmed by applying the appropriate signals on the TMS and TCK inputs and shifting data into and out of the devices on the TDI and TDO pins, respectively. After programming, the IEEE Std. 1149.1 JTAG Test Access Port (TAP) controller state machine must be advanced to the RESET state, which is maintained by external pull-up resistors on the TCK, TMS, and TDI pins. During normal operation, the pull-up resistors prevent the device from entering other modes.

[Figure 3](#) shows the timing waveforms for the IEEE Std. 1149.1 JTAG TAP controller state machine.

Figure 3. JTAG Waveforms for MAX Devices

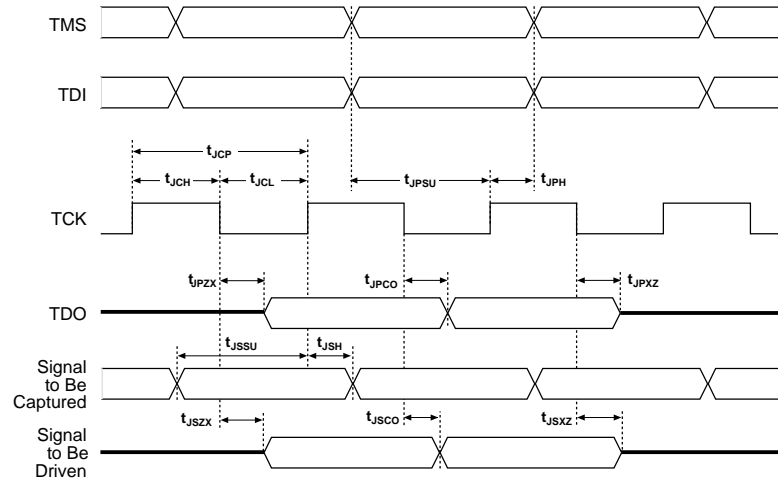


Table 4 shows the JTAG timing parameters and values for ISP-capable MAX devices.

| Table 4. JTAG Timing Parameters & Values for MAX Devices | | | | |
|---------------------------------------------------------------------|------------------------------------------------|------------|------------|-------------|
| Symbol | Parameter | Min | Max | Unit |
| t_{JCP} | TCK clock period | 100 | | ns |
| t_{JCH} | TCK clock high time | 50 | | ns |
| t_{JCL} | TCK clock low time | 50 | | ns |
| t_{JPSU} | JTAG port setup time | 20 | | ns |
| t_{JPH} | JTAG port hold time | 45 | | ns |
| t_{JPCO} | JTAG port clock to output | | 25 | ns |
| t_{JPZX} | JTAG port high impedance to valid output | | 25 | ns |
| t_{JPXZ} | JTAG port valid output to high impedance | | 25 | ns |
| t_{JSSU} | Capture register setup time | 20 | | ns |
| t_{JSH} | Capture register hold time | 45 | | ns |
| t_{JSCO} | Update register clock to output | | 25 | ns |
| t_{JSZX} | Update register high impedance to valid output | | 25 | ns |
| t_{JSXZ} | Update register valid output to high impedance | | 25 | ns |



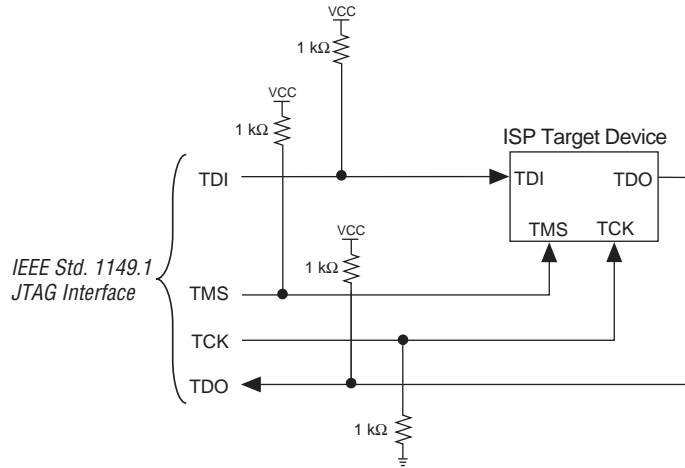
Go to AN 39: IEEE Std.1149.1 (JTAG) Boundary-Scan Testing in Altera Devices for information on the IEEE Std.1149.1 JTAG TAP controller state machine.

Programming ISP-Capable MAX Devices

You can use an IEEE Std.1149.1 JTAG-compatible header to program a single device or a chain of devices, depending on the layout of your PCB.

Single-Device Programming

For PCBs that contain a single ISP-capable MAX device, a JTAG-compatible header—such as the 10-pin BitBlaster or ByteBlasterMV header—can be used to program the device. See [Figure 4](#).

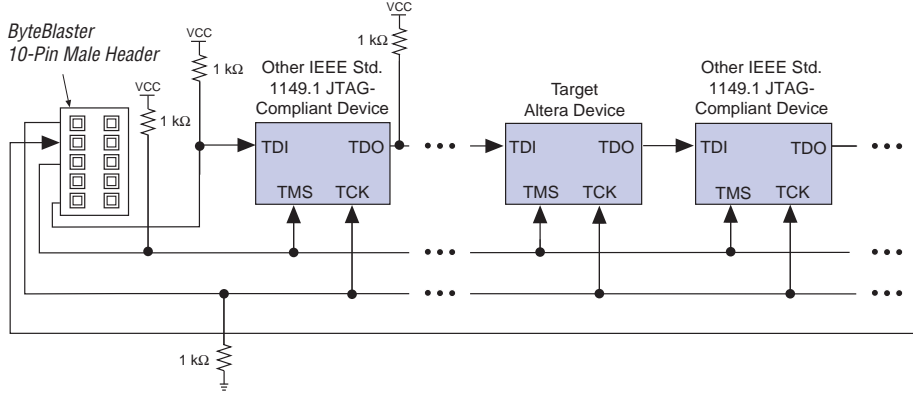
Figure 4. Single-Device Programming

JTAG-Chain Device Programming

When programming a chain of devices, one JTAG-compatible plug, such as a BitBlaster or ByteBlasterMV 10-pin male plug, is connected to several devices. The number of devices in the JTAG chain is limited only by the drive capability of the BitBlaster or ByteBlasterMV download cable. However, when three or more devices are connected in a JTAG chain, Altera recommends buffering the TDO, TCK, TDI, and TMS pins.

JTAG-chain device programming is ideal when the circuit board contains multiple devices, or when the circuit board is tested using JTAG BST. See [Figure 5](#).

Figure 5. JTAG-Chain Device Programming with a BitBlaster or ByteBlasterMV Cable



To program a single ISP-capable MAX device in a JTAG chain, the programming software puts all other devices in the JTAG chain in BYPASS mode. When in BYPASS mode, devices pass programming data from the TDI pin to the TDO pin through a single bypass register. Bypassed devices are not affected internally, thereby enabling the programming software to erase, program, or verify the target device.



Go to AN 39: *IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices* for more information on the BYPASS mode.

Conclusion

ISP-capable MAX devices offer benefits in product design, prototyping, and manufacturing. ISP simplifies the manufacturing flow by allowing the devices to be mounted on a PCB with standard pick-and-place equipment before they are programmed. ISP-capable MAX devices can be programmed by downloading the information via in-circuit testers, embedded processors, or the BitBlaster or ByteBlasterMV download cables. In addition, programming these devices after they are placed on the board eliminates lead damage on high pin-count packages, e.g., quad flat pack (QFP) packages, due to device handling. These devices can also be reprogrammed in the field (i.e., product upgrades can be performed in the field via software or modem).



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