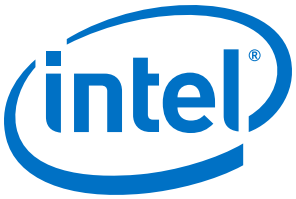

AN 320: Using Intel® FPGA IP Evaluation Mode

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1 AN 320: Using Intel® FPGA IP Evaluation Mode

Intel and strategic IP partners offer a broad portfolio of configurable IP cores optimized for Intel FPGA devices. You can integrate optimized and verified IP cores into your design to shorten design cycles and maximize performance. The Intel® Quartus® Prime software installation includes the Intel FPGA IP library. This library provides many useful IP cores for your production use without the need for an additional license.

Some Intel FPGA IP cores require purchase of a separate license for production use. The Intel FPGA IP Evaluation Mode allows you to evaluate these licensed Intel FPGA IP cores in simulation and hardware, before deciding to purchase a full production IP core license. You can evaluate any of the following with the Intel FPGA IP Evaluation Mode:

- Simulate the behavior of a licensed IP core in your system.
- Verify the functionality, size, and speed of the IP core quickly and easily.
- Generate time-limited device programming files for designs that include IP cores.
- Program a device with your IP core and verify your design in hardware.

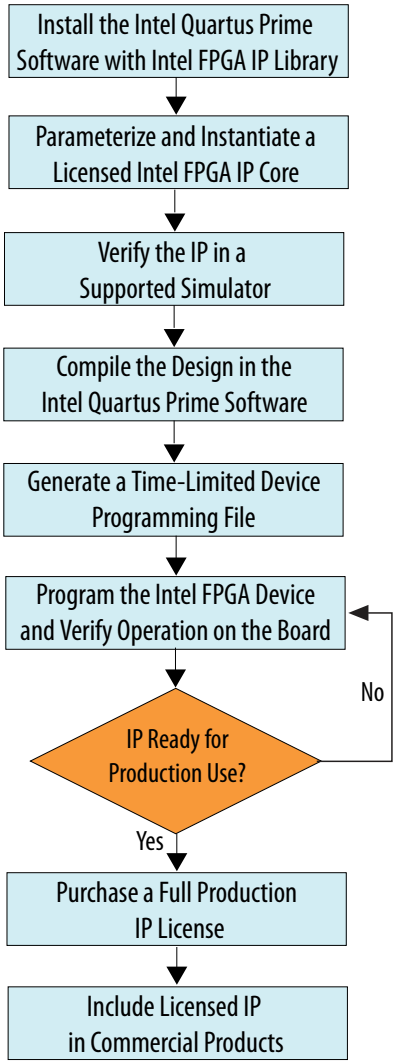
1.1 Intel FPGA IP Evaluation Modes

The Intel FPGA IP Evaluation Mode supports the following two modes:

- Tethered—Allows running the design containing the licensed IP indefinitely with a connection between your board and the host computer. Tethered mode requires a serial joint test action group (JTAG) cable connected between the JTAG port on your board and the host computer, which is running the Intel Quartus Prime Programmer for the duration of the hardware evaluation period. The Programmer only requires a minimum installation of the Intel Quartus Prime software, and requires no Intel Quartus Prime license. The host computer controls the evaluation time by sending a periodic signal to the device via the JTAG port. If all licensed IP cores in the design support tethered mode, the evaluation time runs until any IP core evaluation expires. If all of the IP cores support unlimited evaluation time, the device does not time-out.
- Untethered—Allows running the design containing the licensed IP for a limited time. The IP core reverts to untethered mode if the device disconnects from the host computer running the Intel Quartus Prime software. The IP core also reverts to untethered mode if any other licensed IP core in the design does not support tethered mode.

When the evaluation time expires for any licensed IP in the design, the design stops functioning. All IP cores that use the Intel FPGA IP Evaluation Mode time out simultaneously when any IP core in the design times out. When the evaluation time expires, you must reprogram the FPGA device before continuing hardware verification. To extend use of the IP core for production, purchase a full production license for the IP core.

Figure 1. Intel FPGA IP Evaluation Mode Flow



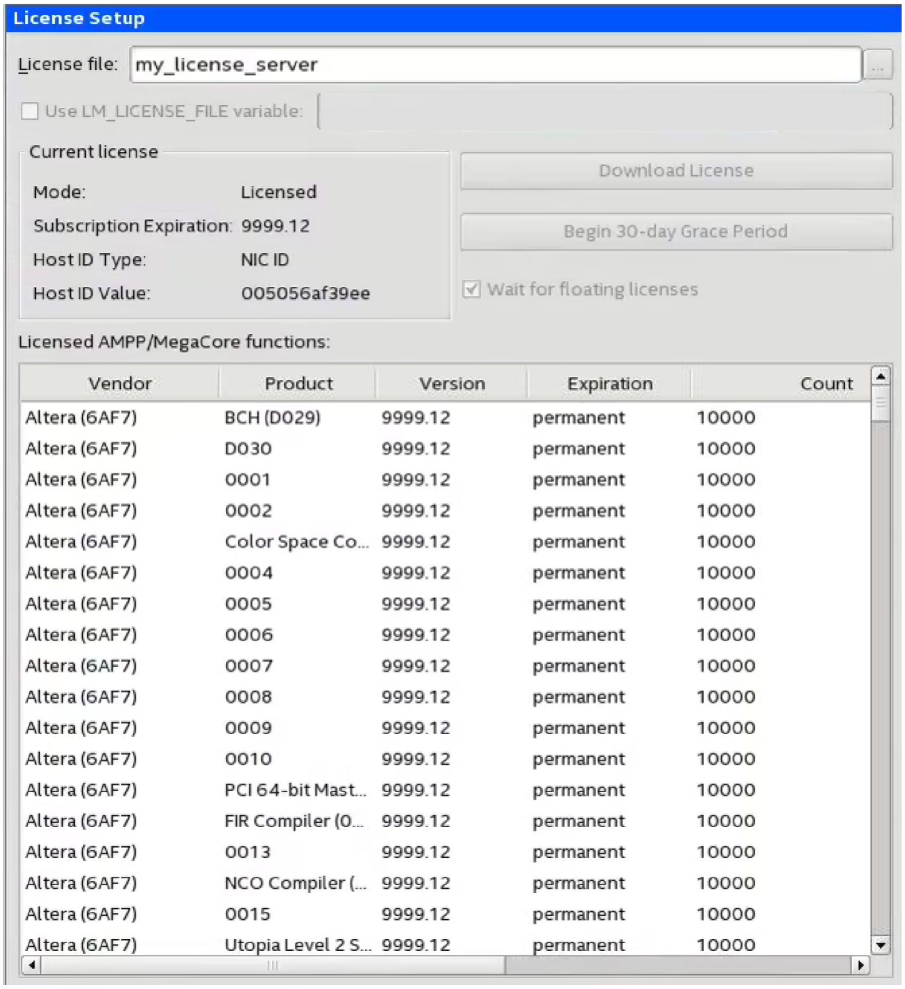
Note: Refer to each IP core's user guide for parameterization steps and implementation details.

1.2 Viewing IP Core License Status

You can view the license type and expiration date of Intel FPGA IP cores in the Intel Quartus Prime software GUI.

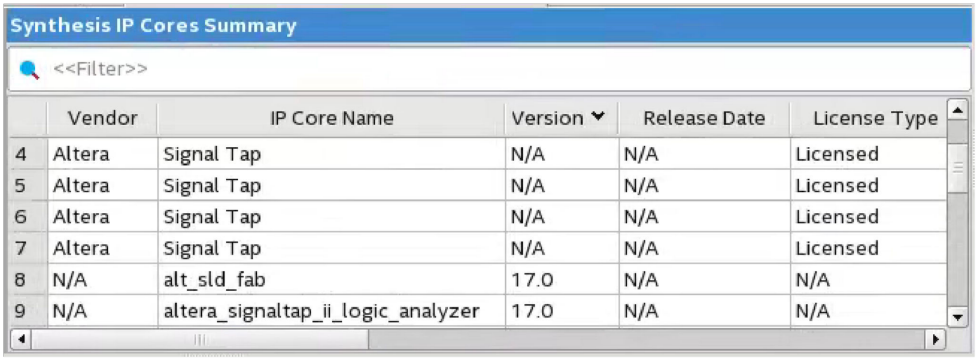
- To view IP and software license and expiration information, click **Tools ➤ License Setup**. The **License Setup** page displays the name, vendor, version, and license expiration date for the IP cores that you install.

Figure 2. License Setup Page



- To view the license type for IP cores in your project, run Analysis & Synthesis, and then view the **Synthesis IP Cores Summary** report. This report displays the name, vendor, version, license type, and other data about the IP cores in your project.

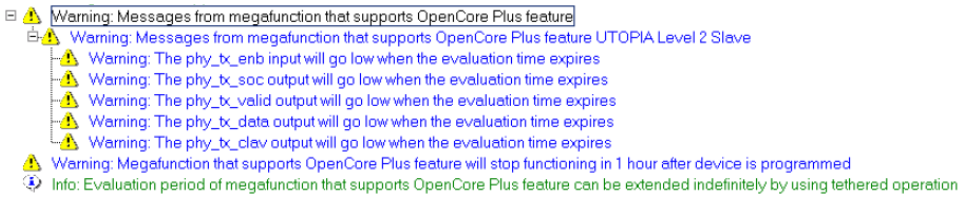
Figure 3. Synthesis IP Cores Summary Report



1.3 Intel FPGA IP Evaluation Mode Messages

The Intel Quartus Prime Compiler generates messages about IP cores under evaluation mode. During compilation, the Compiler reports the soonest, untethered expiration time for all licensed Intel FPGA IP cores in the design. The Compiler also reports the tethered mode evaluation time if all licensed Intel FPGA IP cores in the design support tethered mode.

Figure 4. IP Evaluation Time Limit Messages



Note: The precise time of IP core evaluation timeout depends on the target FPGA device family and operating conditions.

1.4 Licensing Intel FPGA IP Cores

You only need to purchase a full production license for licensed Intel IP cores after you complete hardware testing and are ready to use the IP in production. You must purchase the license and generate a full production license key before you can generate an unrestricted device programming file. During Intel FPGA IP Evaluation Mode, the Compiler only generates a time-limited device programming file (`<project name>_time_limited.sof`) that expires at the time limit.

Intel licenses IP cores on a per-seat, perpetual basis. The license fee includes first-year maintenance and support. You must renew the maintenance contract to receive updates, bug fixes, and technical support beyond the first year. You must purchase a full production license for Intel FPGA IP cores that require a production license, before generating programming files that you may use for an unlimited time. To obtain your production license keys, visit the Self-Service Licensing Center or contact your local Intel FPGA representative.

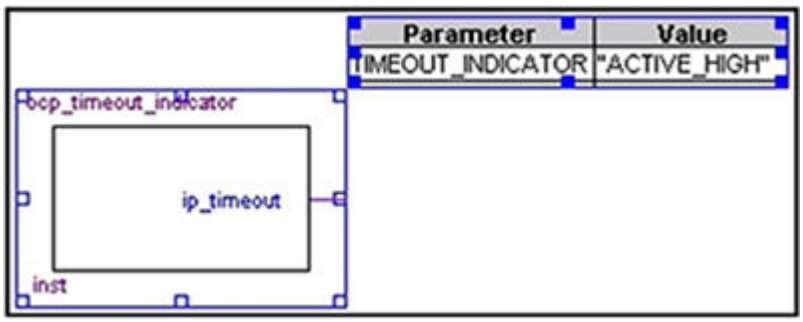
The Intel FPGA Software License Agreements governs the installation and use of licensed IP cores and the Intel Quartus Prime design software and all unlicensed IP cores.

1.5 Evaluation Period Timeout Indicator

The Intel Quartus Prime software installation includes the ocp_timeout_indicator IP block in the `libraries\others\opercore_plus\` directory. You can instantiate this IP block in your design to alert when the device times out.

Specify either an `active_high` or `active_low` polarity of the time-out signal (`ip_timeout`) with the `timeout_indicator` parameter.

Figure 5. OCP_TIMEOUT_INDICATOR IP Block Symbol



Example 1. Timeout Indicator VHDL Component Declaration

```
component ocp_timeout_indicator is
generic
(
TIMEOUT_INDICATOR: string := "ACTIVE_HIGH"
);
port
(
ip_timeout: out std_logic
);
end component ocp_timeout_indicator;
```

Example 2. Timeout Indicator VHDL Instantiation Prototype

```
My_Instance : ocp_timeout_indicator
GENERIC MAP(TIMEOUT_INDICATOR => "ACTIVE_HIGH")
PORT MAP(ip_timeout => My_Output);
```

Example 3. Timeout Indicator Verilog HDL Instantiation Prototype

```
ocp_timeout_indicator my_instance
(.ip_timeout(my_output));
defparam my_instance.TIMEOUT_INDICATOR =
"ACTIVE_HIGH";
```

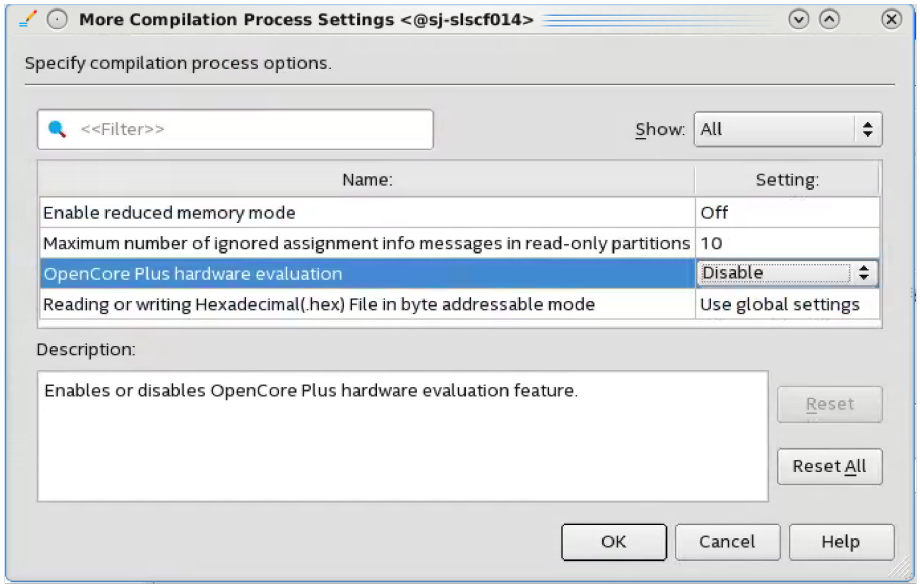
1.6 Disable Intel FPGA IP Evaluation Mode

The Intel FPGA IP Evaluation Mode is enabled by default. Implementation of the Intel FPGA IP Evaluation Mode requires the use of some FPGA device resources. This use of device resources can impact design placement, routing, and timing.

If you are not using Intel FPGA IP Evaluation Mode, and wish to prevent use of these device resources, follow these steps to disable the feature:

1. In the Intel Quartus Prime software, click **Assignments ➤ Settings ➤ Compilation Process Settings**.
2. Click the **More Settings** button.
3. For **OpenCore Plus hardware evaluation**, select **Disable**.

Figure 6. Disable IP Evaluation Mode



1.7 Using Intel FPGA IP Evaluation Mode in Teams (Intel Quartus Prime Standard Edition)

The Intel Quartus Prime Standard Edition software supports Intel FPGA IP Evaluation Mode in a team with distributed design tasks. The Intel FPGA IP Evaluation Mode allows individual designers to simulate and hardware test a design containing licensed IP, without requiring licenses for each designer. However, ultimately you must generate the production-ready FPGA programming file on a machine with an available full production license for all licensed IP cores in the design.

The most flexible methodology for distributed work flows is for every designer to have a production license for all IP included in their portion of the design. However, you can use the Intel Quartus Prime Standard Edition incremental compilation feature to temporarily avoid the licensing requirement by following these steps on any machine with an Intel Quartus Prime Standard Edition license:

1. Click **Assignments ➤ Settings ➤ Compilation Process Settings ➤ More Settings**, and disable **OpenCore plus hardware evaluation**.

   Note: You cannot use incremental compilation to compile a portion of your design that contains licensed IP in evaluation mode, and then import that design as a pre-compiled module to another machine that has a production license for the IP.

2. To compile the design, click **Processing ➤ Start Compilation**.
3. To export the compilation results as a design partition, click **Project ➤ Export Design Partition**. The Intel Quartus Prime software generates an Intel Quartus Prime Exported Partition File (`.qxp`) in the project directory.
4. To generate a full production, non-time-limited device programming file for the exported partition, you must import the partition to a project with access to a full production license for all licensed IP core in the design. Click **Project ➤ Import Design Partitions** to import a design partition.

1.8 Document Revision History

Table 1. Document Revision History

Date	Changes
2017.07.15	• Changed references from OpenCore Plus to Intel FPGA IP Evaluation Mode. • Updated for latest Intel branding conventions. • Differentiated between Intel Quartus Prime Pro Edition and Intel Quartus Prime Standard Edition features.
2007.11.08	Added section on IP evaluation in teams.
2007.09.15	Removed references to unsupported LogicLock® flow.
2007.05.08	Updated steps for disabling evaluation mode.
2003.10.15	Initial document release.