Understanding I/O Output Timing for Altera Devices

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Introduction

This application note describes the output timing parameters for Altera® devices, explains how Altera defines t_{CO} results, and presents techniques for calculating the output timing for your system. In addition, a sample DDR2 interface link is presented and analyzed for calculating output timing.

Detailed timing information is available in the device handbooks and from the Quartus® II software. The timing information in the handbooks presumes a sample design and is specific to that one implementation for that device. Your implementation may be different, so you should obtain timing data that directly applies to your system by using the values reported by the Quartus II timing analyzer (TAN) or TimeQuest.

When dealing with output timing parameters such as t_{CO}, the Quartus II software is only aware of the FPGA-related timing components. The Quartus II software does not have information on the PCB or the receiving device. It is important to understand exactly what the t_{CO} result parameters represent and to understand how to use the timing reported by the Quartus II software to determine complete system timing.

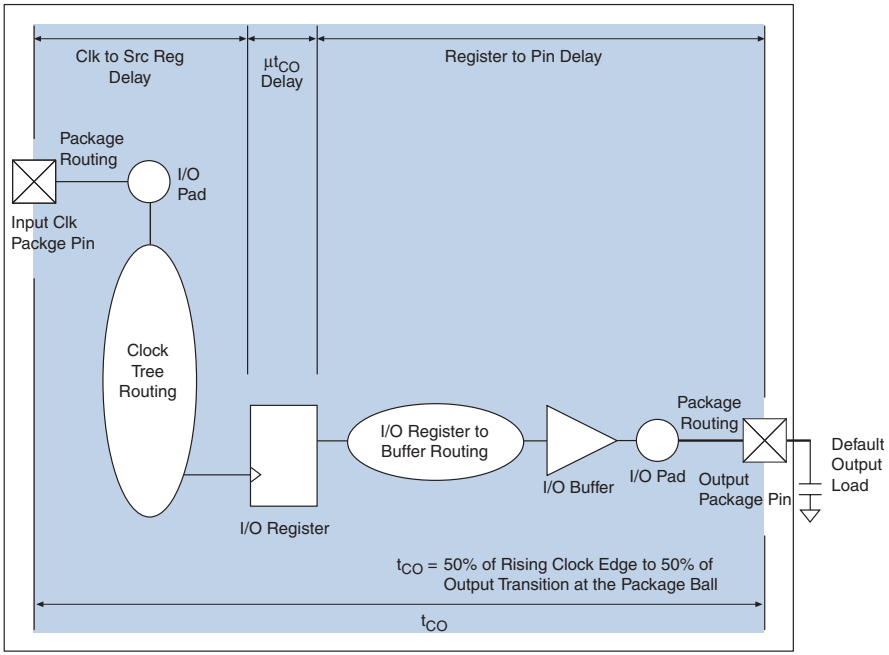
t_{CO} Timing Parameter

The t_{CO} parameter, commonly referred to as the "clock-to-out" delay parameter, specifies the time it takes for a valid signal to appear on the output of a register or I/O after a clock transition. For Altera devices, t_{CO} is the time delay from when a clock signal reaches the 50% input threshold on an input pin to when an output signal crosses the 50% switching threshold at the ball of an output pin. The following equation shows how the Quartus II software calculates t_{CO}:

t_{CO} = *<clock to source register delay>* + *<micro clock to output delay>* + *<register to pin delay>*

Figure 1 illustrates the path for the t_{CO} timing parameter in the Quartus II software.

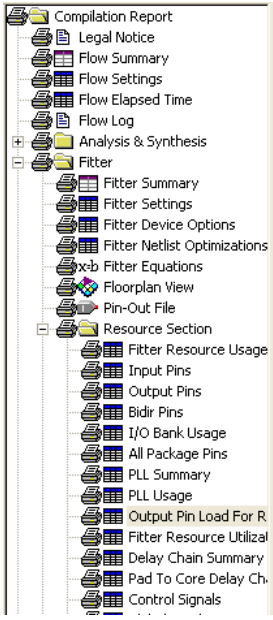
Figure 1. t_{CO} Timing Path



Default Output Load Conditions for t_{CO} Values

The Quartus II software reports the t_{CO} timing for a given pin with a default reference load, as defined on the Output Pin Load for Reported t_{CO} page (Compilation Report > Fitter > Resource Section) shown in Figure 2.

Figure 2. Output Pin Load Page From the Quartus II software



Output Pin Load For Reported TCO

	I/O Standard	Load	Termination Resistance
1	LVTTL	0 pF	Not Available
2	LVCMOS	0 pF	Not Available
3	2.5 V	0 pF	Not Available
4	1.8 V	0 pF	Not Available
5	1.5 V	0 pF	Not Available
6	3.3-V PCI	10 pF	25 Ohm
7	3.3-V PCI-X	10 pF	25 Ohm
8	SSTL-2 Class I	0 pF	50 Ohm (Parallel), 25 Ohm (Serial)
9	SSTL-2 Class II	0 pF	25 Ohm (Parallel), 25 Ohm (Serial)
10	SSTL-18 Class I	0 pF	50 Ohm (Parallel), 25 Ohm (Serial)
11	SSTL-18 Class II	0 pF	25 Ohm (Parallel), 25 Ohm (Serial)
12	1.5-V HSTL Class I	0 pF	50 Ohm
13	1.5-V HSTL Class II	0 pF	25 Ohm
14	1.8-V HSTL Class I	0 pF	50 Ohm
15	1.8-V HSTL Class II	0 pF	25 Ohm
16	Differential SSTL-2	0 pF	(See SSTL-2)
17	Differential SSTL-2 Class II	0 pF	(See SSTL-2 Class II)
18	Differential 1.8-V SSTL Class I	0 pF	(See 1.8-V SSTL Class I)
19	Differential 1.8-V SSTL Class II	0 pF	(See 1.8-V SSTL Class II)
20	Differential 1.5-V HSTL	0 pF	(See 1.5-V HSTL Class I)
21	Differential 1.5-V HSTL Class II	0 pF	(See 1.5-V HSTL Class II)
22	Differential 1.8-V HSTL Class I	0 pF	(See 1.8-V HSTL Class I)
23	Differential 1.8-V HSTL Class II	0 pF	(See 1.8-V HSTL Class II)
24	LVDS	0 pF	100 Ohm

Calculating Output Timing

This section discusses three methods for calculating output timing for your system:

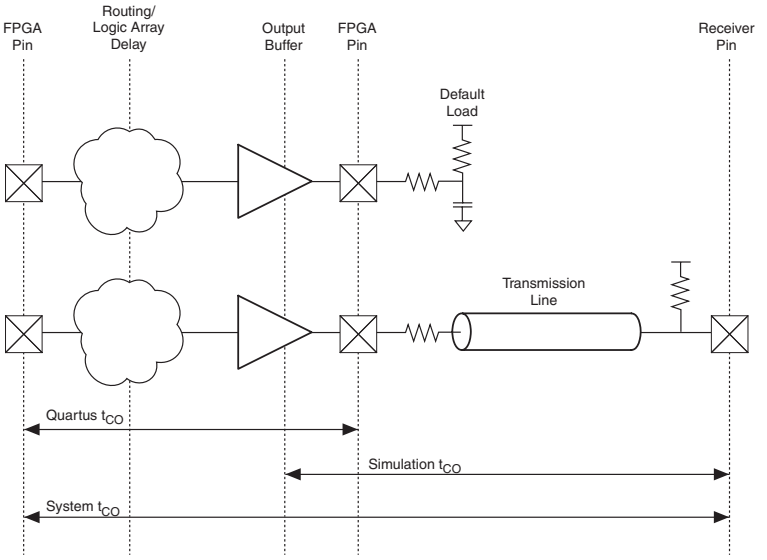
- Default t_{CO} (method 1)
- Hand PCB delay analysis (method 2)
- I/O model simulation analysis (method 3)

When performing system-timing analysis, you should look at the timing delay from one device to the next, not just the t_{CO} parameter for the driving device. Methods 2 and 3 describe techniques to calculate the timing delay between devices. The method descriptions use three terms to describe the techniques:

- The Quartus II t_{CO} refers to the t_{CO} value reported by the Quartus II TAN for the default load conditions
- Simulation t_{CO} refers to the time delay from the output buffer to the receiver pin, reported by IBIS or HSPICE simulation tools
- System t_{CO} refers to the time delay from the clock transition at the input pin to the signal transition at the receiver pin of the receiving device

Figure 3 provides a graphical representation of the three terms.

Figure 3. t_{CO} Definitions



Method 1: Default t_{CO}

This method involves using the default t_{CO} reported by the Quartus II timing analyzer or the output timing values shown in the device handbook. In most cases, the default load conditions do not match what is present in your system. If your system has different loading conditions than those expected by the Quartus II software (refer to Figure 2), the t_{CO} values reported by the TAN do not match the t_{CO} values observed in your system.

The Quartus II software is unaware of what is beyond the output pin, so it cannot accurately report the t_{CO}. Therefore, you should not use the default t_{CO} method to calculate output timing if accuracy is important in your analysis.

Method 2: Hand PCB Delay Analysis

This method involves specifying the output load conditions in the Quartus II software and using rule-of-thumb calculations to determine the output timing for your system or system t_{CO}. The Quartus II software allows you to specify the output load for each individual output pin to

describe the loading conditions. By specifying the receiver's input pin capacitance, the TAN is able to model the effect of the receiver on the t_{CO} for the respective output pin. You can set the custom load value in the Quartus II software by using the Output Pin Load assignment in the Assignment Editor (Assignments Menu).

You can calculate the system t_{CO} for a given link between the output driver and input receiver by using the new t_{CO} and rule-of-thumb copper delay calculations (for example, 166 ps per inch for FR4 trace). This method provides you with a good first-order estimate for system t_{CO} and provides a much more accurate value compared to relying on the default Quartus II t_{CO} value. It is a good alternative if you do not have access to an IBIS or HSPICE simulation tool to perform I/O model simulation analysis.

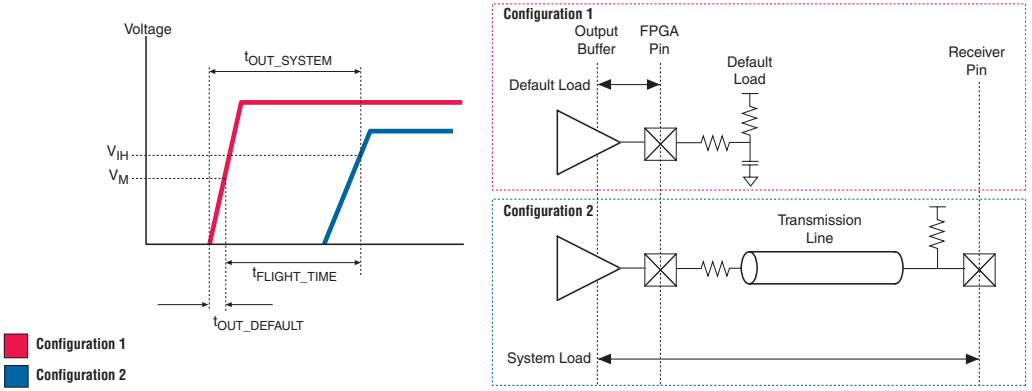
Method 3: I/O Model Simulation Analysis

This method involves performing simulations on the output driver, transmission line, and input receiver using I/O models. Simulations using IBIS and HSPICE I/O models allow you to predict the effects of the receiver, transmission lines, connectors, termination resistors, and so on on the output signal. Although these electrical models are predominantly used for signal integrity analysis, they can provide valuable delay information through interconnects and transmission lines. You can calculate the system t_{CO} for a given link using the simulation t_{CO} in conjunction with the Quartus II t_{CO}.

In Figure 4, if you simply add up the Quartus II t_{CO} and simulation t_{CO}, there is some overlap from the output buffer to the output pin. This combined value would be a pessimistic value for system t_{CO} because you count the delay from the output buffer to the output pin twice. The following two simulation configurations remove this overlap value from your system t_{CO} calculations:

- Simulation with default load (configuration 1)
- Simulation with actual system load (configuration 2)

Figure 4. I/O Model Simulations



In configuration 1, set up a simulation with the output buffer and the default load. Note the time delay from the output to the V_M, or the measured voltage point, typically 50% of the output signal swing. Refer to this value as $t_{OUT\_DEFAULT}$, as shown in Figure 4. The reference load values and the V_M values are available in the operating conditions section from the handbook or data sheet for the device, or on the Output Pin Load for Reported t_{CO} page (Compilation Report > Fitter > Resource Section) shown in Figure 2 on page 3.

For configuration 2, set up a simulation with the output buffer, the system load, including the transmission line, interconnects, termination, and the receiver input. Note the time delay from the output to the minimum V_{IH} level specified by the I/O standard in use by the receiver input pin. The V_{IH} level indicates when the receiver reaches a logic "high" level. You must use the maximum V_{IL} level when running falling edge simulations. Refer to this value as t_{OUT_SYSTEM}, as shown in Figure 4, or as system t_{CO}.

You can use the two t_{OUT} values to calculate the flight time. The flight time does not include the overlap value, so it provides the true system t_{CO}.

$$\text{Flight time} = t_{OUT\_SYSTEM} - t_{OUT\_DEFAULT}$$

$$\text{System } t_{CO} = \text{Quartus II } t_{CO} + \text{flight time}$$

It is important to use the worst-case process model, voltage, and temperature conditions in these simulations to calculate the worst-case t_{CO} value. The I/O model simulation analysis method provides the most accurate way to calculate system t_{CO}.

Case Study

The examples in this section use the three methods described in this application note to calculate the system t_{CO}.

The case study looks at a Stratix® II device driving to a DDR2 SDRAM memory device. An EP2S60F1020C3 SSTL18-C1 output drives the DQ pin of the Micron MT47H32M8 device. The HyperLynx simulation file in Figure 5 shows the link between the two devices.

Figure 5. HyperLynx System Load Simulation Setup

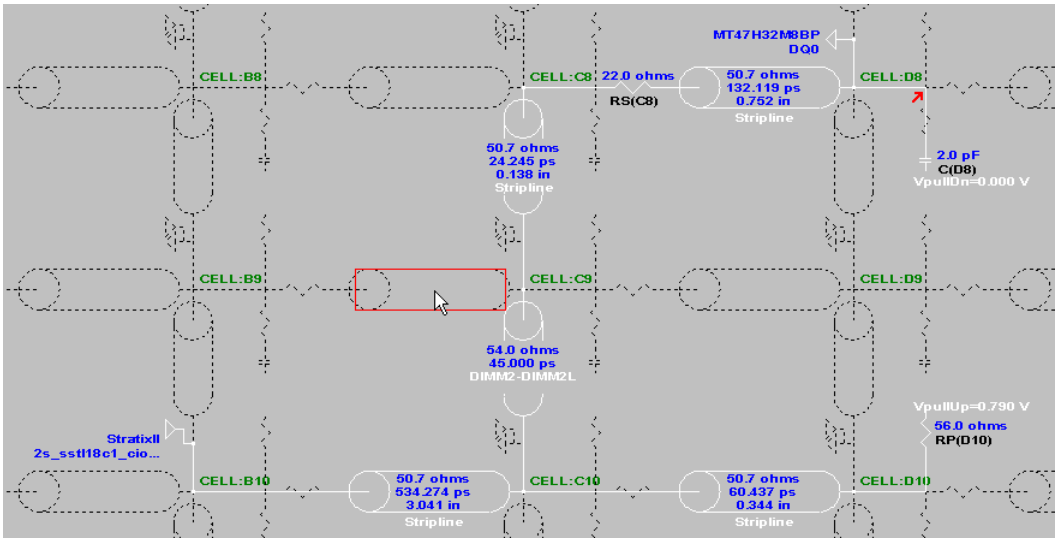
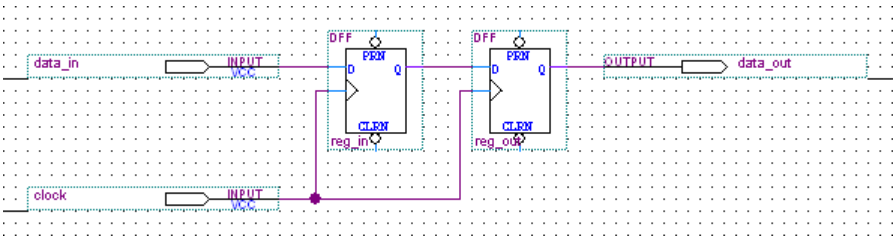


Figure 6 illustrates the simple Quartus II design used to obtain timing information for this case study.

Figure 6. Quartus II data_out Test Design



Method 1 Example

Using method 1, compile the design shown in Figure 6. The Quartus II software assumes an output load of 0 pF by default, if an output load value is not specified. After compilation, the Quartus II TAN reports the t_{CO} as 4.160 ns for the `data_out` pin. This value is the baseline t_{CO} or the Quartus II t_{CO}.

Method 2 Example

To calculate the system t_{CO} using method 2, choose the Output Pin Load option with an output pin load of 6 pF in the Quartus II software and rerun timing analysis. The 6 pF represents the 4 pF pin capacitance of the DQ pin, as described in the Micron data sheet, and a 2 pF capacitance representing the package of the MT47H32M8 device. The new t_{CO} reported by the Quartus II TAN with the output pin load specified as 6 pF is 4.286 ns.

Next, determine the length of the various stripline components to calculate the delay. Adding up the three stripline lengths from Figure 5 on page 7 gives you (3.041 + 0.138 + 0.752) = 3.931 inches.

Using rule-of-thumb calculations for an FR-4 copper trace (length * 166 ps/inch) gives you 3.931 inches * 166 ps/inch = 0.653 ns.

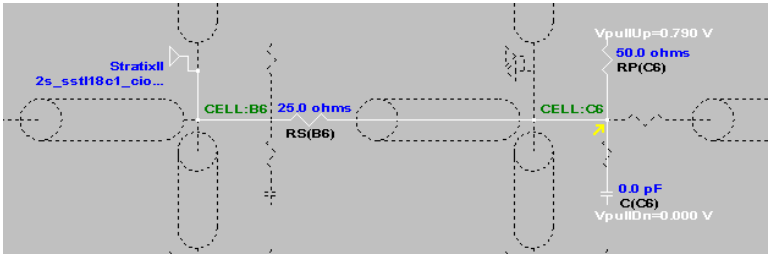
Adding the delay value of 0.653 ns to the t_{CO} value of 4.286 ns gives a system t_{CO} value of 4.939 ns.

This analysis does not take into account the delay and effect through the DIMM connector or model the change of the resistor values (25 -> 22 Ω and 50 -> 56 Ω) from the expected values.

Method 3 Example

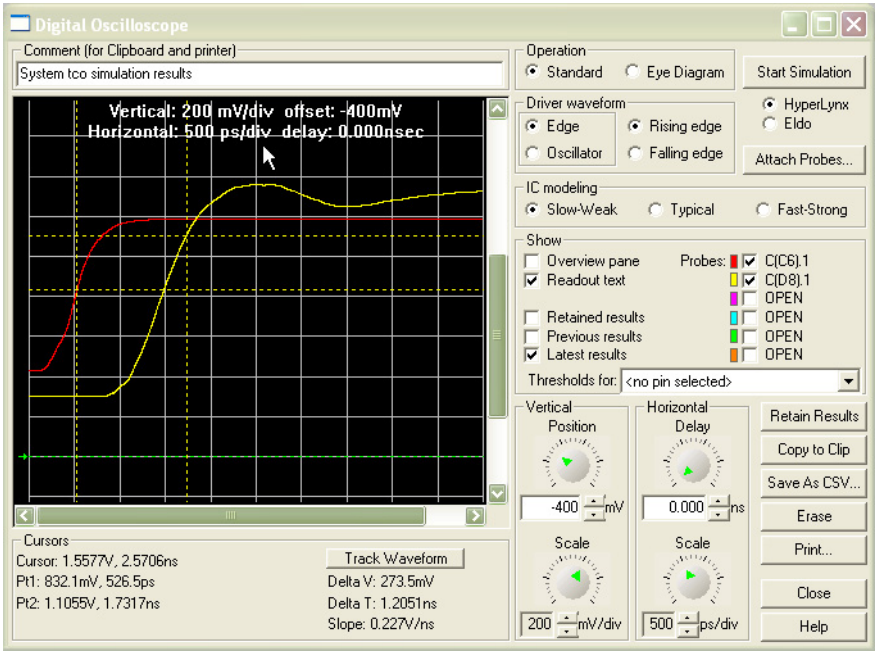
This example for method 3 uses the HyperLynx IBIS simulation tool from Mentor Graphics®. To calculate system t_{CO} using method 3, set up two simulations, one with the system load and the other with the default load, as shown in Figures 5 and 7, respectively.

Figure 7. HyperLynx Default Load Simulation Setup



Using the HyperLynx tool, you can quickly observe the flight time between the default and system load case using a V_M of 0.83 V and V_{IH} of 1.105 V. You can obtain the values for V_M and V_{IH} from the *Stratix II Device Handbook*. Figure 8 shows the HyperLynx simulation results and a flight time of 1.205 ns (Delta T value in the Cursors area).

Figure 8. HyperLynx Simulation Results for Default & System Loads



Adding the flight time to the baseline t_{CO} gives a result of 4.160 ns + 1.205 ns = 5.365 ns, the system t_{CO} between the driver and receiver.

Table 1 summarizes the t_{CO} values obtained using the different methods.

Table 1. t_{CO} Results

Method	t_{CO}
Default t_{CO}	4.160 ns
Hand PCB delay analysis	4.939 ns
I/O model simulation analysis	5.365 ns

From the results you can see that method 1 underestimates the system t_{CO} results value by over 1 ns compared to method 3. Again, you should not use method 1, because it does not take into account the effect from the output load and the transmission line. You can also see that method 3 provides a slightly more conservative estimate for system t_{CO} results compared to method 2. Method 3 more accurately represents the components between the Stratix II driver and the Micron receiver. In addition, it calculates the delay to the minimum V_{IH} level, which provides the minimum point when the receiver begins to switch.

If you have access to I/O model simulation tools such as HyperLynx from Mentor Graphics , method 3 provides the most accurate results for system t_{CO}. If you are unable to run simulations, method 2 is a good alternative.

Conclusion

The concepts discussed in this application note show how to use the output timing parameters reported by the Quartus II software. It also provided methods to help you perform timing analysis for your system. It is important to understand what the timing parameters represent and choose the appropriate method to obtain accurate t_{CO} results.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
www.altera.com
Applications Hotline: (800) 800-EPLD
Literature Services: literature@altera.com