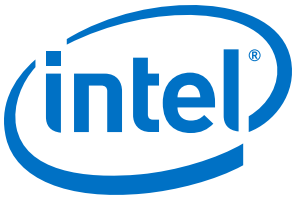

AN 447: Interfacing Intel® FPGA Devices with 3.3/3.0/2.5 V LVTTL/ LVCMOS I/O Systems

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Contents

Interfacing Intel® FPGA Devices with 3.3/3.0/2.5 V LVTTL/LVCMOS I/O Systems

Transmission line effects can cause a large voltage deviation at the receiver. This deviation can damage the input buffer, especially for I/O standards without termination, such as LVTTL or LVCMOS.

To manage signal integrity issues and protect the input pin, follow the guidelines in this document if you interface 3.3 V, 3.0 V, 2.5 V LVTTL or LVCMOS I/O systems with these Intel device families:

- Cyclone® III
- Cyclone IV
- Intel Cyclone 10 LP
- Intel MAX® 10

Note: In this document, the term "supported Intel devices" refers to devices in the listed device families only.

To ensure device reliability and proper operation, you must design the I/O interfaces within the specifications recommended by the guidelines in this document.

Receiver Level Requirements

You must address signal integrity issues if you use the supported Intel devices in 3.3 V, 3.0 V, 2.5 V LVTTL or LVCMOS interfaces. Otherwise, you may not meet the devices' absolute maximum DC input voltage and maximum allowed overshoot/ undershoot voltage requirements.

The supported Intel devices have one V_{CCIO} voltage level per I/O bank. Additionally, the devices can also have driver input voltage levels for input signaling. Not all combinations of V_{CCIO} and driver input voltage require attention with regards to the maximum input voltage.

Follow the guidelines in this document to manage the voltage overshoot and input requirements.

Figure 1. Simulation Waveform of 3.3 V LVTTL Output Interfacing 3.3 V LVTTL Input

This figure shows an exampe of a supported Intel device with 3.3 V LVTTL interface at the highest drive current setting and without termination. The simulation shows that an excessively large overshoot is present at the receiver when the I/O is driven from a high current driver through an unterminated transmission line.

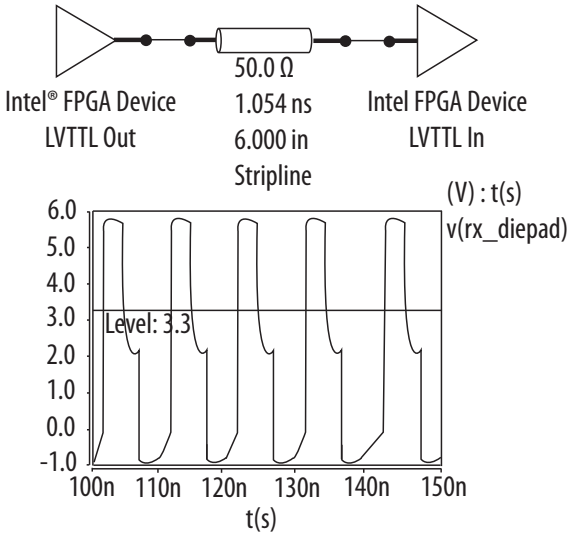


Table 1. Receiver Level Requirements for 3.3/3.0/2.5 V LVTTL/LVCMOS

This table lists the recommended actions for the I/O interface voltage combinations that require attention.

Supported Intel Device Receiver Bank V_{CCIO}	LVTTL/LVCMOS Driver Voltage Level		
	2.5 V	3.0 V	3.3 V
2.5 V	No action required	Disable diode and apply series termination or use driver selection table. The devices' I/O pin is overdriven by a higher external voltage. You must meet the DC current specification of the diode. Alternatively, you can apply series termination to manage voltage overshoot. In such cases, Intel recommends that you disable the diode due to the possible presence of a high DC current.	
3.0 V	No action required	No action required	No action required
3.3 V	Apply series termination or use driver selection table. Diode clamped voltage can still exceed the maximum DC and AC specifications due to the high V_{CCIO} voltage level of the bank in which the I/O resides. You must manage the voltage overshoot. You can leave the diode enabled without concern for the DC current as the I/O pin is not overdriven.		

- The conditions and actions in the preceding table apply only when the supported Intel device's I/O pin is assigned as input, bidirectional, or tristated output using the 3.3/3.0/2.5 V LVTTL/LVCMOS I/O standards. No attention is required when the device's I/O pin is used as output only.
- The Intel Quartus® Prime software enables the PCI-clamp diode on this pin for each of these conditions by default.
- Other I/O standards, such as 1.8 V, 1.5 V, or 1.2 V LVTTL or LVCMOS, 3.0 V PCI or PCI-X, voltage-referenced, and differential I/O standards, do not require attention on the maximum input voltage.

For more information about the absolute maximum DC input voltage and maximum allowed overshoot/undershoot voltage for the device families covered in this document, refer to the related information.

Related Links

- Cyclone III Device Datasheet
- Cyclone III LS Device Datasheet
- Cyclone IV Device Datasheet
- Intel Cyclone 10 LP Device Datasheet
- Intel Intel MAX 10 FPGA Device Datasheet

Guideline: Use Internal PCI Clamp Diode on the Pin

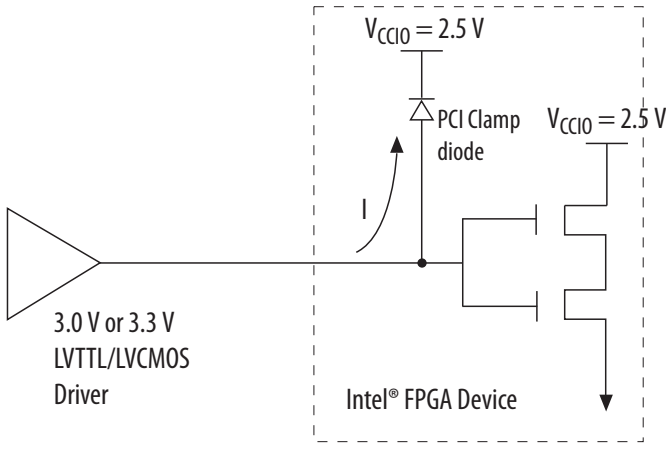
The supported Intel devices provide an optional PCI clamp diode for each I/O pin. You can use this diode to protect I/O pins against voltage overshoot.

By default, if the assigned input, bidirectional, or tristated output pins use 3.3 V, 3.0 V, or 2.5 V LVTTL or LVCMOS I/O standards, the Intel Quartus Prime software enables the PCI clamp diode on the pin.

The PCI clamp diode can sufficiently clamp voltage overshoot to within the DC and AC input voltage specifications when the bank supply voltage (V_{CCIO}) is 2.5 V or 3.0 V. You can clamp the voltage for a 3.3 V V_{CCIO} to a level that exceeds the DC and AC input voltage specifications with ± 5% supply voltage tolerance. The clamped voltage is expressed as the sum of the supply voltage (V_{CCIO}) and the diode forward voltage.

Note: Dual-purpose configuration pins support the diode in user mode if the specific pins are not used as configuration pins for the selected configuration scheme. Dedicated configuration pins do not support the on-chip diode.

Figure 2. PCI Clamp Diode in Supported Intel Devices



The PCI clamp diode in the supported Intel devices can support a maximum of 10 mA DC current. The diode sinks the DC current when driven by a voltage level that exceeds the bank V_{CCIO} plus the diode forward voltage. You must take the DC sink into consideration current when you interface a 2.5 V V_{CCIO} receiver on the supported Intel device with 3.0 V and 3.3 V LVTTL or LVCMOS I/O systems.

Note: The 10 mA DC current limit refers to the current that the diode sinks and not the drive strength of the driver. This limit is only applicable when the PCI clamp diode is enabled and when the 2.5 V receiver of the supported Intel device interfaces with 3.0 V or 3.3 V LVTTL or LVCMOS I/O systems.

If you disable the diode in the Intel Quartus Prime software, ensure that the interface meets the DC and AC specifications.

If your system has the flexibility to accommodate a selection of driver strengths, you can also use the driver selection guideline to select the appropriate driver without using termination.

Related Links

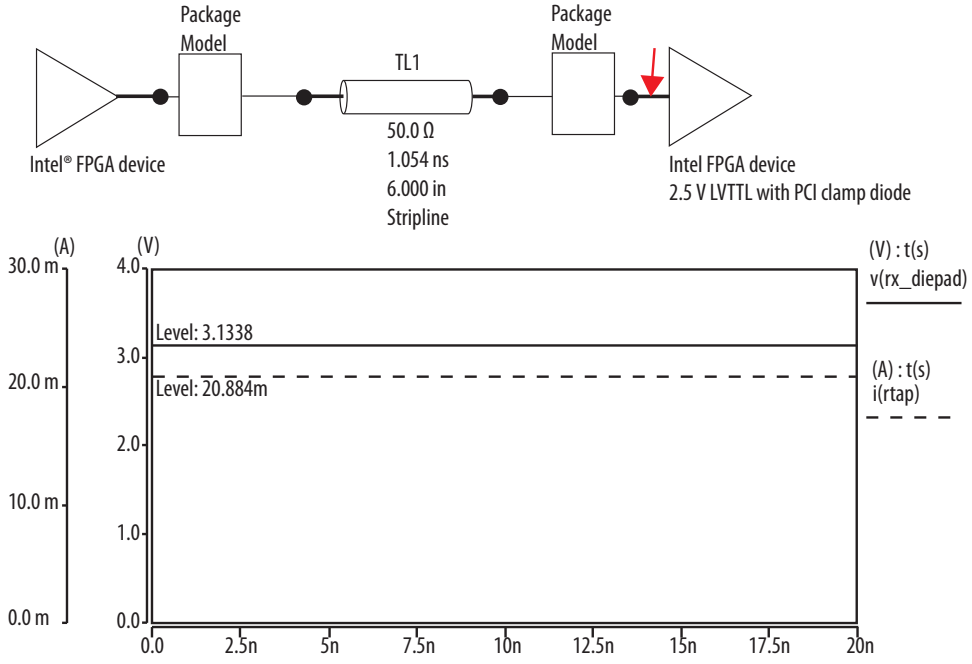
- Volume 2: Design Implementation and Optimization, Intel Quartus Prime Handbook
  Provides information about disabling the PCI clamp diode using the assignment editor.
- Guideline: Select Appropriate Driver on page 10

Measuring DC Current with PCI Clamp Diode

The PCI clamp diode is forward-biased when the driver voltage level exceeds the V_{CCIO} plus diode forward voltage.

DC current exists when the diode is forward-biased. The amount of DC current depends on the driver output impedance, driver and receiver supply voltage, diode forward voltage, and a small resistance intrinsic to the transmission line.

Figure 3. Simulation Setup and Result to Determine DC Current that Flows into the PCI Clamp Diode



1. Set up the driver to drive static logic-high signal into the receiver of the supported Intel device with the PCI clamp diode enabled.
2. Apply the maximum supply voltage at the driver and the minimum V_{CCIO} at the receiver of the supported Intel device for the highest DC current.
3. Take the current measurement from the die pad of the supported Intel device—denoted by the red pointer in the preceding figure.

   You can obtain current measurements using a small sense resistor (in mili-Ω) placed in series to the transmission line.

As shown in the preceding figure, a 20.88 mA DC current sink in the PCI clamp diode is measured. The result significantly exceeds the 10 mA maximum current supported by the diode.

Related Links

Receiver Level Requirements on page 3
Provides guidelines to interface 3.3 V, 3.0 V, or 2.5 V LVTTL or LVCMOS I/O standards with supported Intel FPGA devices.

Guideline: Use Series Termination Resistor

Transmission line effects that cause large voltage deviation at the receiver are associated with impedance mismatch between the driver and transmission line. You can use a series termination resistor placed physically close to the driver to match the total driver impedance to transmission line impedance.

You can significantly reduce voltage overshoot by matching the impedance of the driver to the characteristic impedance of the transmission line.

If the driver device manufacturer specifies the driver buffer output impedance, you can use the following equation to determine the apropriate series termination value:

$R_{driver}+R_{series}\approx Z_0$

Where:

- R_{driver} represents the intrinsic impedance of the driver
- R_{series} represents the resistance of the external series resistor

If the output impedance value of the driver is not available, you can simulate an IBIS model for the driver to determind the appropriate series termination resistor value for the interface.

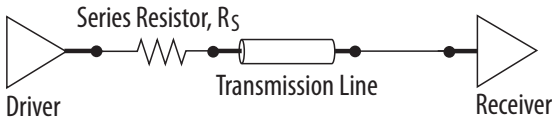
Some drivers offer series on-chip termination (OCT) to minimize impedance mismatch to the transmission line. You can select a driver with R_{driver} that closely matches the transmission line impedance in such cases. OCT provides sufficient impedance matching without the expense of additional external component.

Note: OCT affects the edge rates of the transmitted signal. You must evaluate if the timing impact causes a performance degradation of the interface.

Selecting Appropriate Series Termination Resistor Value

The series termination scheme works by introducing a resistor placed in series between the driver and receiver. The driver impedance and series resistance become the total effective driver impedance. The transmission line impedance has to match the driver impedance to minimize reflection and manage overshoot.

Figure 4. Series Termination Scheme



You must perform a simulation to determine the suitable series resistor value for your interface within the allowable tolerance condition. Choosing the appropriate resistor value for series termination is important:

- If the resistance is too small, the termination may not effectively reduce or eliminate the overshoot.
- If the resistance is too large, the driver may not sufficiently drive the transmission line and it can result in a stair-step response.

Example of Determining Series Termination Resistor Value

This example shows how to determine the value of the series termination resistor to manage the voltage overshoot effectively. The example uses the terminator wizard feature in the HyperLynx simulation software by Mentor Graphics Corporation. You can explore other appropriate methods via simulation to determine a suitable series resistor value for your interface.

In this example, an Intel FPGA with 3.3-V LVTTL 16 mA ouput is driven to a Cyclone III 2.5-V LVTTL input. You can disable the diode and apply the series termination, or use the driver selection reference.

Figure 5. Intel FPGA 3.3 V LVTTL 16 mA Interfacing with Cyclone III 2.5 V LVTTL

Set up the desired interface in the Schematic Editor as represented in this figure and run the terminator wizard.

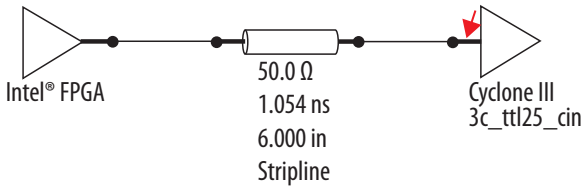


Figure 6. Terminator Wizard Results From HyperLynx Simulation Software by Mentor Graphics Corporation

The Terminator Wizard results suggest adding a 33 Ω series resistance.

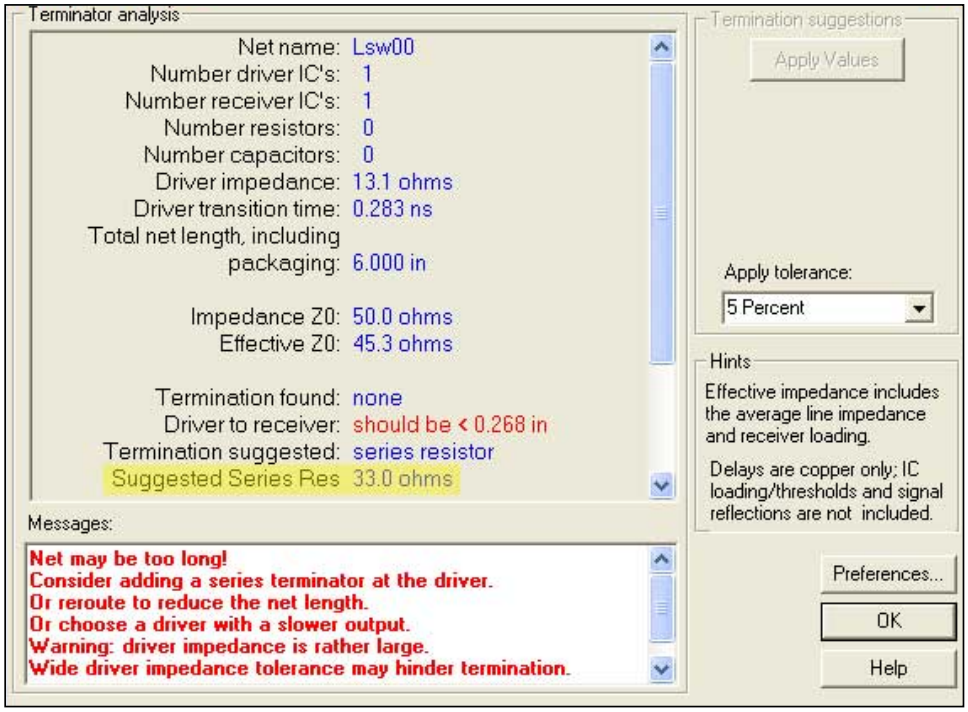


Figure 7. Intel FPGA 3.3 V LVTTL 16 mA Interfacing with Cyclone III 2.5 V LVTTL with Recommended 33.0 Ω Series Termination Resistor

The suggested 33 Ω series resistance is applied close to the Intel FPGA driver.

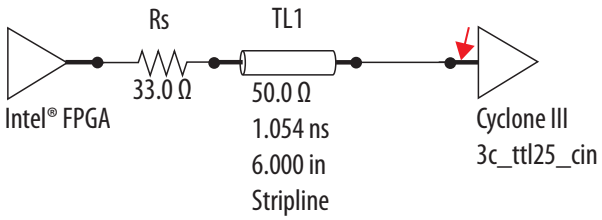
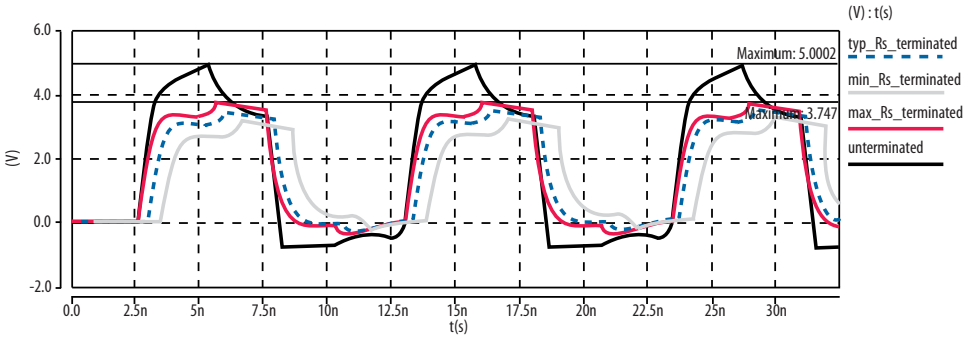


Figure 8. Simulation Waveforms Comparing Terminated and Non-Terminated Interface Across Typical, Minimum, and Maximum Conditions

The new setup in this example is evaluated at different allowable conditions to ensure that DC and AC specifications are met and to identify the impact of introducing the resistor in the interface.



Related Links

Driver Selection Reference on page 10

Guideline: Select Appropriate Driver

The output characteristics of a driver determines how much overshoot voltage is seen at the receiver when the interface is not terminated. You can address signal integrity concerns in your interface by selecting the appropriate driver.

You must select a driver that meets the current limits of the supported Intel device at the appropriate points in the I/V curve. You can obtain the I/V curve of the driver from the IBIS file provided by the device manufacturer.

You can also use slew rate control, if it is available on the driver, to address signal integrity concerns. Slew rate control allows you to reduce the edge rate of the output signal to help control voltage overshoot at the receiver. You must perform simulations to ensure that the specifications are met when using the slew rate feature.

Driver Selection Reference

A driver can drive a receiver without termination even if it produces overshoot, undershoot, and ringing in the interface as long as it meets two key specifications: voltage threshold and maximum input voltage of the receiver device.

Conformance to the voltage threshold specification ensures the correct logic-low and logic-high switching. On the other hand, conformance to the maximum DC and AC input specifications ensures the reliability of the receiver device in the system over an extended period.

A driver can drive to a supported Intel device without requiring termination if the measured current of the driver is less than the current limit in the preceding table for the desired interface setup. The limits ensure that the DC and AC maximum input voltage specifications and maximum DC current for diode are met, if the driver current value is within the limits.

Table 2. V_{OH} Level for Each I/O Standard

This table lists the current limits that are the maximum allowable driver current values at the V_{OH} level.

Driver I/O Standard	V_{OH} Level
2.5 V LVTTL	2.0 V
3.0 V LVTTL	2.4 V
3.0 V LVCMOS	V_{CCIO} – 0.2 V
3.3 V LVTTL	2.4 V
3.3 V LVCMOS	V_{CCIO} – 0.2 V

The current limits in the following table takes into account the DC and AC requirements of the receiver, and the use of the PCI clamp diode. You can use the values as measurements to identify if a driver meets the input specifications of the supported Intel device for the target I/O standard. Using these values, you can select the appropriate driver without performing simulation.

Table 3. Maximum Allowed Current Metrics Required to Drive Supported Intel Devices without Termination

This table lists the maximum current limits of the drivers that interface with the supported Intel devices without termination in each I/O interface combination.

Driver Voltage Level	Receiver Bank V_{CCIO}(V)(1)		
	2.5 ± 5%	3.0 ± 5%	3.3 ± 5%
2.5 V LVTTL	No maximum limit	No maximum limit	48 mA
3.0 V LVTTL	26 mA	No maximum limit	26 mA
3.0 V LVCMOS	8 mA	No maximum limit	8 mA
3.3 V LVTTL	15 mA (30 mA)(2)	No maximum limit	30 mA
3.3 V LVCMOS	4 mA (8 mA)(2)	No maximum limit	12 mA

- The pull-up I/V curve represents the current and voltage behavior of the driver when it is sourcing logic-high.
- Take the measurement at the driver maximum allowable operating condition, which is at a low temperature and high supply voltage, to account for the worst possible overshoot condition.
- The current limit does not represent the current strength of a driver associated with a particular I/O standard.
- You must perform the measurement on the I/V curve at the maximum condition.

(1) The Intel Quartus Prime software enables the PCI clamp diode for pins assigned as 3.3 V, 3.0 V, or 2.5 V LVTTL or LVCMOS I/O standards by default.

(2) The value in brackets is the current limit for the driver if you disable the PCI clamp diode. For this combination, disabling the diode offers the driver slightly more margin. For other combinations, enabling the diode offers the driver better margin.

Current Limits Measurement Examples

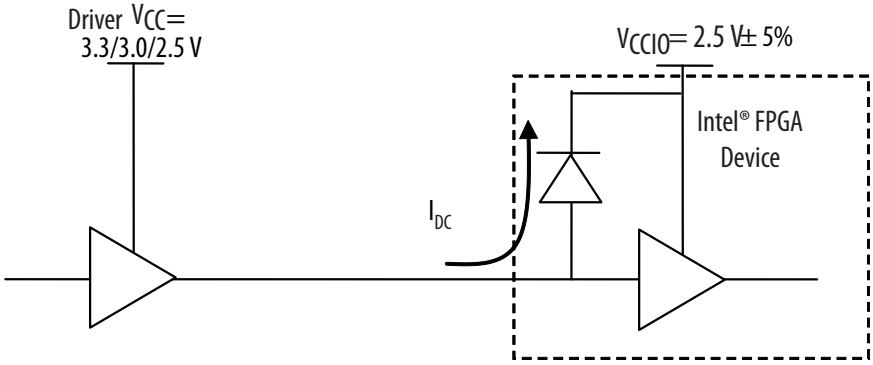
The following examples use the driver selection reference to evaluate an interface from a Cyclone series device to the Intel Cyclone 10 LP, Cyclone IV, or Cyclone III device receiver using the 3.3 V LVTTL I/O standard via unterminated transmission line.

For the interface evaluation in these examples, the current strength of the Cyclone device is 8 mA.

Example 1. Input Setup with 2.5 V V_{CCIO}

The supported Intel device's on-chip PCI diode starts to sink the DC current I_{DC} when driven by a steady state voltage greater than the sum of the supported Intel device's V_{CCIO} and diode forward voltage in the following figure. The diode is forward-biased when the driver's V_{CC} is 3.3 V or 3.0 V and the I_{DC} must not exceed 10 mA.

Figure 9. Supported Intel Device Input Setup with 2.5 V V_{CCIO}

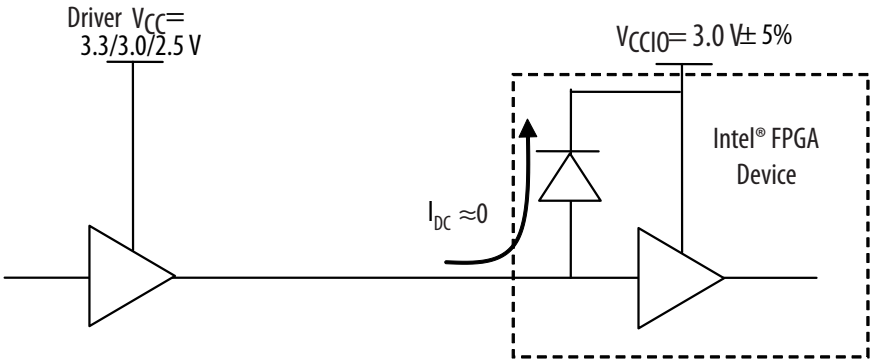


The amount of I_{DC} through the diode is determined by the potential voltage difference between the driver and the supported Intel device's pin, and the current capability of the driver. The diode can limit the transient voltage level to below the specification limit when the driver's V_{CC} is 2.5 V—effectively limiting it to 3.325 V with the assumption that V_{CCIO} is 2.625 V and diode forward voltage is 0.7 V.

Example 2. Input Setup with 3.0 V V_{CCIO}

The diode might not be forward-biased even when the driver's V_{CC} is 3.3 V as the potential voltage difference between the driver's V_{CC} and the supported Intel device's V_{CCIO} is less than the diode forward voltage. Therefore, there is no concern on I_{DC} through the diode when driven with an input voltage level of 3.3 V, 3.0 V, or 2.5 V as shown in the following figure.

Figure 10. Supported Intel Device Input Setup with 3.0 V V_{CCIO}

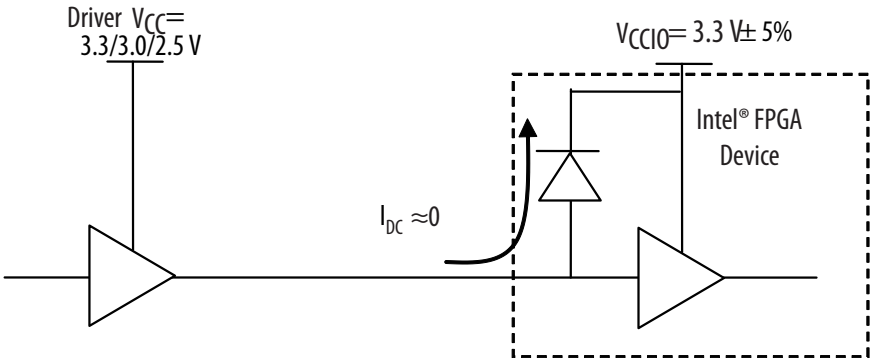


The forward-bias of the diode occurs only momentarily during overshoot conditions to clamp the overshoot voltage level. In such cases, the diode is effective in limiting the transient voltage level to below the specification limit—effectively limiting it to 3.85 V with the assumption that V_{CCIO} is 3.15 V and diode forward voltage is 0.7 V.

Example 3. Input Setup with 3.3 V V_{CCIO}

I_{DC} is almost zero at a steady input voltage level as the diode might not be forward-biased as shown in the setup in the following figure. At a higher V_{CC} level of the driver, such as 3.465 V, the diode clamps transient voltage level at 4.165 V with the assumption that diode forward voltage is 0.7 V.

Figure 11. Supported Intel Device Input Setup with 3.3 V V_{CCIO}



The use of a lower driver current capability reduces the voltage overshoot level. You must ensure that the duration of the overshoot is below these limits:

- For Intel Cyclone 10 LP, Cyclone IV, and Cyclone III devices, the percentage of high time for an overshoot of 4.15 V can be as high as 18.52% over a 10-year period.
- For Intel MAX 10 devices, the percentage of high time for an overshoot of 4.17 V can be as high as 11.7% over a 10-year period.

Related Links

Driver Selection Reference on page 10

Evaluating Interface Using Driver Selection Method

An easy and convenient method to determine the current limits is to perform the measurement on the driver pull-up I/V curve in the IBIS model.

1. Obtain the IBIS model for the driver.

   The model used as the driver is `1c_ttl33_io_d8` from the `cyclone.ibs` file. You can perform a DC sweep simulation on the HSPICE model and set the buffer to drive logic-high if the IBIS model is not available for the driver.

2. Open the IBIS file using the HyperLynx Visual IBIS Editor.

   The editor provides a graphical view of IBIS model data, which provides a measurement of the I/V values in graphical format.

3. Run the graphical view mode.

   a. Navigate to the `1c_ttl33_io_d8` model data from tree-view pane on the left column in the editor.

   b. Right-click on the model denoted by `[Model] 1c_ttl33_io_d8` and select **View Data**.
   A dialog box appears with multiple tabs for each data characteristic available for the model.

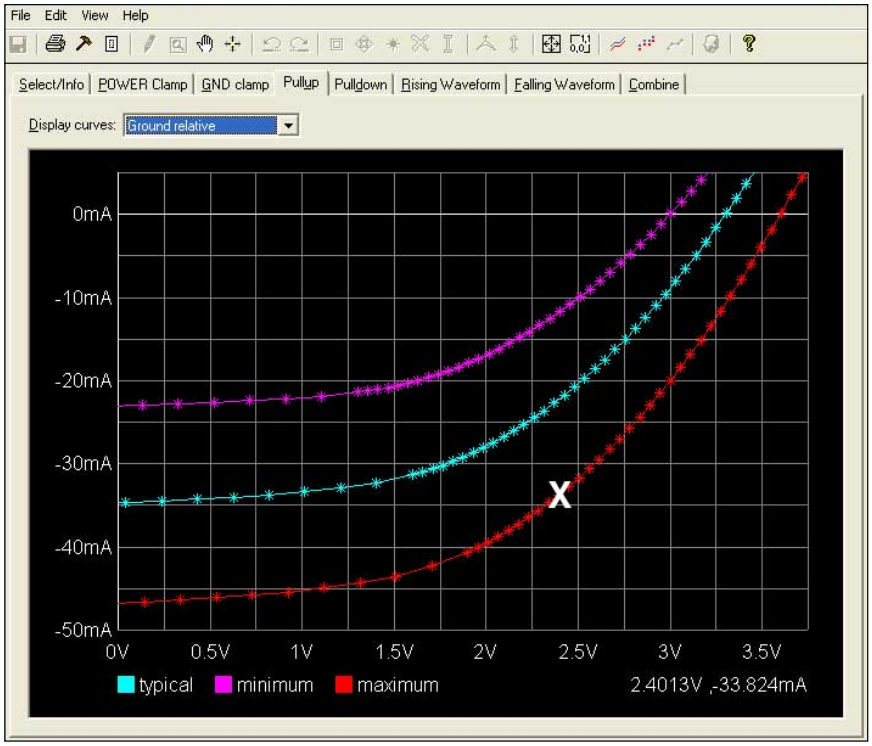
4. Select the pull-up I/V curve.

   a. Select the **Pullup** tab in the dialog window.

   b. In the **Display Curves** list, select **Ground relative**.

Figure 12. Current Limit Measurement for IBIS Pull-Up Data Using Graphical Viewer HyperLynx Visual IBIS Editor

In the figure, the measured current is 33.8 mA.



5. Identify the appropriate V_{OH} level and perform the current measurement.

   Based on the driver selection reference, the V_{OH} for the 3.3 V LVTTL driver is 2.4 V (see related information). Look for the maximum I/V curve and make the visual approximation current measurement at 2.4 V.

6. Identify allowed current limit.

   Based on the maximum allowed current metrics for the supported Intel device (see related information), the current limit is 30 mA for a 3.3 V LVTTL driver to a 3.3 V receiver bank of a supported Intel device. The measured current exceeds the maximum allowed current limit.

From the preceding example, a Cyclone device operating as the driver at 3.3 V LVTTL with 8 mA setting is not able to drive directly the supported Intel device's input at 3.3 V VCCIO supply without termination. The Cyclone device might not meet the DC and AC input voltage specification of the supported Intel devices.

To solve the problem, you can apply series termination according to the recommended receiver level requirements.

Related Links

- Driver Selection Reference on page 10
- Altera IBIS Models
  Provides the IBIS models for all Intel FPGA devices.
- Receiver Level Requirements on page 3

Interface Current between Supported Intel Devices

The supported Intel devices can drive into each other without termination for certain drive strengths using the 3.3 V, 3.0 V, or 2.5 V LVTTL or LVCMOS I/O standards.

Table 4. Interface Current Between Supported Intel Devices Without Additional Solution

In this table, "Yes" means that you can drive into the supported Intel device receiver unterminated—with the I/O standard drive strengh and corresponding bank V_{CCIO}—without violating the DC and AC input voltage specifications.

Driver I/O Standard	Drive Strength	Receiver Bank V_{CCIO}(V)[3]		
		2.5 ± 5%	3.0 ± 5%	3.3 ± 5%
2.5 V LVTTL	4 mA	Yes	Yes	Yes
	8 mA	Yes	Yes	Yes
	12 mA	Yes	Yes	—
	16 mA	Yes	Yes	—
3.0 V LVTTL	4 mA	Yes	Yes	Yes
	8 mA	Yes	Yes	Yes
	12 mA	—	Yes	—
	16 mA	—	Yes	—
3.0 V LVCMOS	4 mA	Yes	Yes	Yes
	8 mA	—	Yes	—
	12 mA	—	Yes	—
	16 mA	—	Yes	—
3.3 V LVTTL	4 mA	Yes	Yes	Yes
	8 mA	[4]	Yes	Yes
3.3 V LVCMOS	2 mA	[4]	Yes	Yes

(3) The Intel Quartus Prime software enables the PCI clamp diode for pins assigned as 3.3 V, 3.0 V, or 2.5 V LVTTL or LVCMOS I/O standards by default.

(4) With the PCI clamp diode enabled, the supported Intel devices—at this I/O standard, drive strength, and receiver bank V_{CCIO} combination—cannot drive each other unterminated. To use this combination without violating the specifications, disable the PCI clamp diode.

Document Revision History for AN 447: Interfacing Intel FPGA Devices with 3.3/3.0/2.5 V LVTTL/LVCMOS I/O Systems

Date	Version	Changes
November 2017	2017.11.06	• Added support for Intel Cyclone 10 LP devices. • Rebranded as Intel. • Changed instances of *Quartus II* to *Intel Quartus Prime*. • Updated all instances of "Cyclone II" to "Intel FPGA".
May 2016	2016.05.30	Corrected an error in the table listing the maximum allowed current metrics required to drive the supported devices without termination. The text in the last row has been corrected from "3.0 V LVCMOS" to "3.3 V LVCMOS".
December 2014	2014.12.15	• Added support for MAX 10 devices. • Restructured and rewritten the document to improve clarity and for easier reference. • Updated template.
November 2009	2.0	• Updated all Cyclone IV device references. • Removed "Introduction" heading. • Removed "Referenced Documents" section.
June 2009	1.2	• Updated to include Cyclone III LS devices information. — Updated "Introduction" on page 1. — Updated "Background" on page 1. — Updated "Design Guideline" on page 2. — Updated Table 1 on page 2, Table 3 on page 10, Table 4 on page 14. — Updated "PCI-Clamp Diode" on page 3. — Updated "Termination" on page 4. — Updated "Conclusion" on page 5. — Updated "Appendix A: DC Current Measurement with PCI-Clamp Diode" on page 5, "Appendix C: Driver Selection Table and Measurement Method" on page 9, "Appendix D: Cyclone III Device Family to Cyclone III Device Family Interface Matrix" on page 14. — Updated Figure 2 on page 5, Figure 10 on page 10, Figure 11 on page 11, Figure 12 on page 12. — Updated "Referenced Documents" on page 14.
April 2008	1.1	• Added Figure 10, Figure 11, and Figure 12. • Added new note on configuration pins under PCI-Clamp Diode section. • Added new paragraph under Appendix C: Driver Selection Table and Measurement Method section.
March 2007	1.0	Initial release.