

Introduction

Use of the on-chip termination (OCT) scheme in Stratix[®] III devices eliminates the need for external series or parallel termination resistors and simplifies the design of a PCB. Stratix III devices support calibrated on-chip series, parallel and dynamic termination in all I/O banks for single-ended I/O standards. OCT calibration allows you to establish an optimal termination value that compensates impedance change due to temperature and voltage fluctuation. You can enable Stratix III devices calibration by user-controlled signals during device operation or by default during device configuration.

This application note describes how to implement OCT calibration in Stratix III devices. It describes calibrated R_S (series) and R_T (parallel) termination implementations on unidirectional pins and dynamic termination implementations on bidirectional pins in designs such as DDR and DDR2 external memory interfaces. Use this application note in conjunction with the following literature:

- *Stratix III Device I/O Features* chapter in volume1 of the *Stratix III Device Handbook*
- *ALTIOBUF Megafunction User Guide*
- *ALTOCT Megafunction User Guide*

In the Quartus[®] II software version 7.2 and later versions, the OCT calibration block (OCT Calibration Block and Termination Clock Block are used interchangeably throughout this document. The Quartus II software uses “Termination Control Block” terminology) can be instantiated using the MegaWizard[®] Plug-In Manager. This application note and the design examples illustrate OCT calibration block use in power-up mode and user mode, and their association with I/O pins. The application note discusses the following topics:

- OCT calibration in power-up mode with an example design
- OCT calibration in user mode with example designs
- Design considerations that system designers must consider when selecting calibrated OCT feature in Stratix III devices

OCT Calibration Modes

Stratix III devices support R_S and R_T OCT in all I/O banks. OCT calibration can occur in either power-up mode or user mode.

Power-Up Mode OCT Calibration

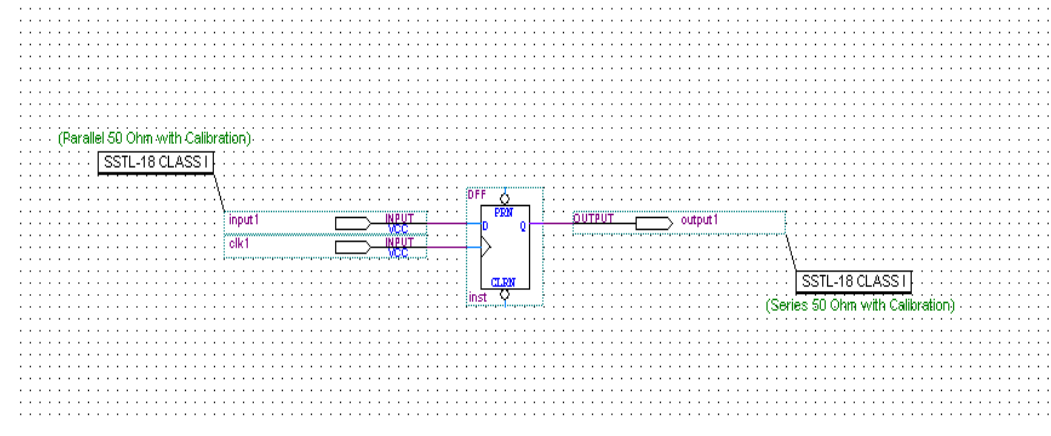
In power-up mode, OCT calibration is automatically performed at power-up before user mode transition for I/Os connected to an OCT calibration block.

The Quartus II software automatically instantiates a power-up mode OCT calibration block if you enable it in the Assignment Editor.

Design Example

This example illustrates calibrated OCT on input and output pins in power-up mode. [Figure 1](#) shows a schematic representation of the power-up mode OCT calibration design.

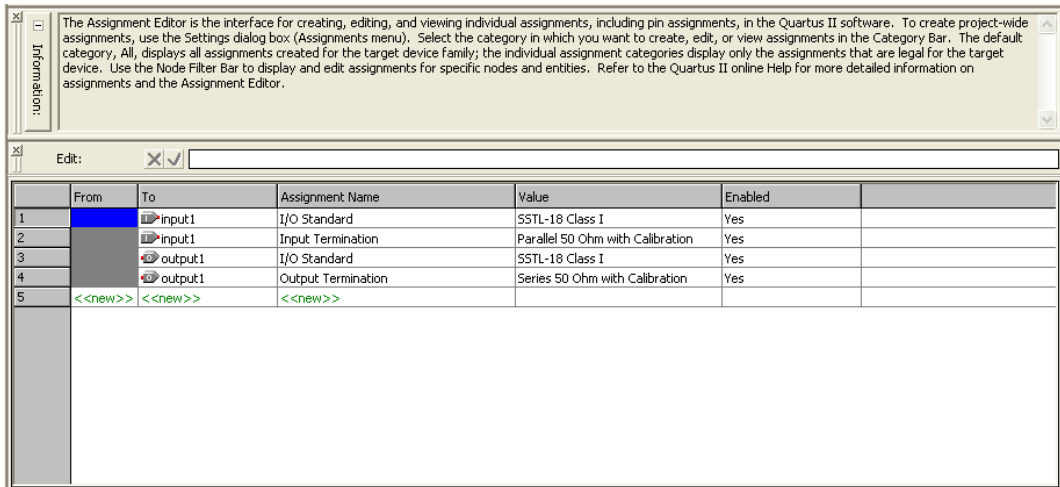
Figure 1. Block Diagram: Power-Up Mode Calibration



The following steps describe the design flow for the design:

1. Using the Assignment Editor in Quartus II, assign the I/O standard. For this design, assign **SSTL-18 Class I** to the input1 and output1 pins (see [Figure 2](#)).

Figure 2. Assignment Editor in the Quartus II Software: Power-Up Mode



2. The two termination related assignments in the Quartus II software for Stratix III devices are INPUT_TERMINATION and OUTPUT_TERMINATION. In the Assignment Editor, assign input termination with value **Parallel 50 Ohm with Calibration** to the input1 pin and output termination with value **Series 50 Ohm with Calibration** to the output1 pin.
3. Compile the design.
4. The report file for input and output pins shows bank location of the OCT calibration block used (see Figures 3 and 4).

Figure 3. Compilation Report for Input Pins in Power-Up Mode

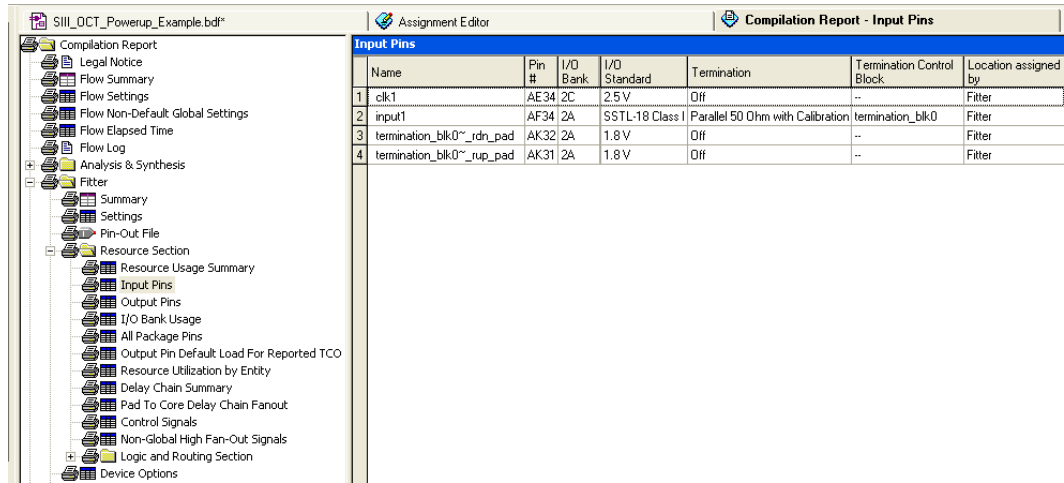
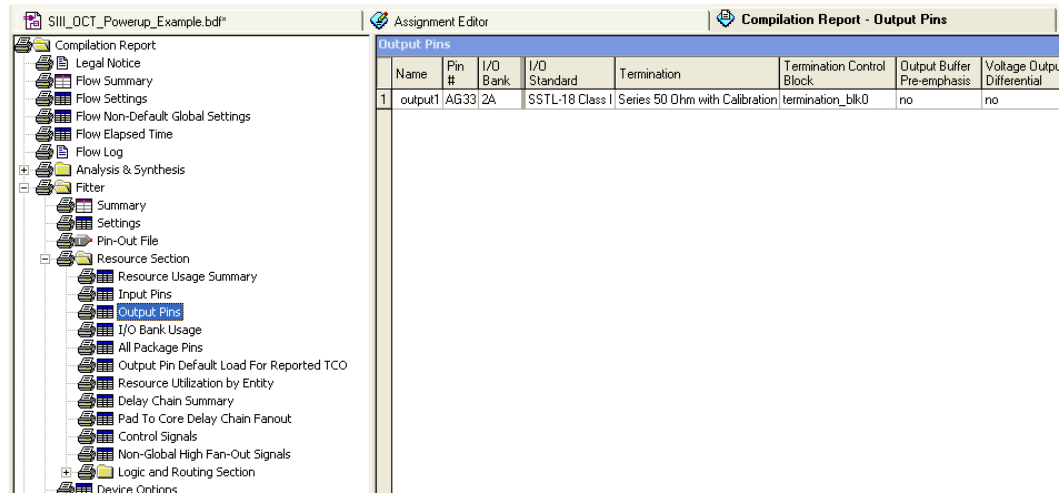


Figure 4. Compilation Report for Output Pins in Power-Up Mode



User Mode OCT Calibration

User-mode calibration allows you to dynamically control OCT calibration after the device is configured. If there are temperature or voltage changes, you can recalibrate to maintain a tight tolerance on OCT. There is no limit to the number of times you can calibrate in user-mode.

If there are temperature and voltage changes, you can determine the OCT variation with the following equation:

$$R_{OCT} = R_{CAL} \left(1 + \frac{dR}{dT} \times \Delta T + \frac{dR}{dV} \times \Delta V \right)$$

R_{OCT} is the resistance value of on-chip termination without recalibration calculated for a given voltage and temperature change.

R_{CAL} is the calibrated on-chip termination at power-up.

$\frac{dR}{dV}$ is the OCT variation with voltage.

$\frac{dR}{dT}$ is the OCT variation with temperature.

ΔV is the change in V_{CCIO} voltage.

ΔT is the change in temperature.



For calibration accuracy, dR/dT , and dR/dV values, refer to the *DC and Switching Characteristics of Stratix III Devices* chapter in volume 2 of the *Stratix III Device Handbook*.

The following example explains how to use the previous equation to determine if recalibration is required.

In this example, $V_{CCIO} = 3.0V$ and $OCT R_S = 50\Omega$ are used for $50\text{-}\Omega$ internal series termination with calibration.

The min/max R_{CAL} at the time of calibration is:

$$(OCTR_S \pm (OCTR_S * \% \text{ calibration accuracy}) = 50 \pm (50 * 0.05) = 52.2\Omega \text{ (max) or } 47.5\Omega \text{ (min)})$$



Refer to the Stratix III On-Chip Termination Calibration Accuracy Specifications table in the *DC and Switching Characteristics of Stratix III Devices* chapter in volume 2 of the *Stratix III Device Handbook*.

Assume a temperature change of $\Delta T = 5^{\circ}\text{C}$ and a voltage change of $\Delta V = 50 \text{ mV}$.

$$\begin{aligned} R_{\text{OCT}} &= 52.5 (1 + (0.294/100) * 5 + (0.029/100) * 150) \\ &= 52.5 (1 + 0.0147 + 0.0145) \\ &= 52.5 (1.0292) \\ &= 54.033\Omega \end{aligned}$$

In this case, OCT recalibration can be used to bring back the value within $\pm 5\%$ tolerance.

Example Design

The ALTOCT megafunction in the Quartus II software provides support for calibrated OCT on Stratix III devices. The ALTOCT megafunction is required to control arbitration logic necessary to configure OCT calibration blocks in the design.



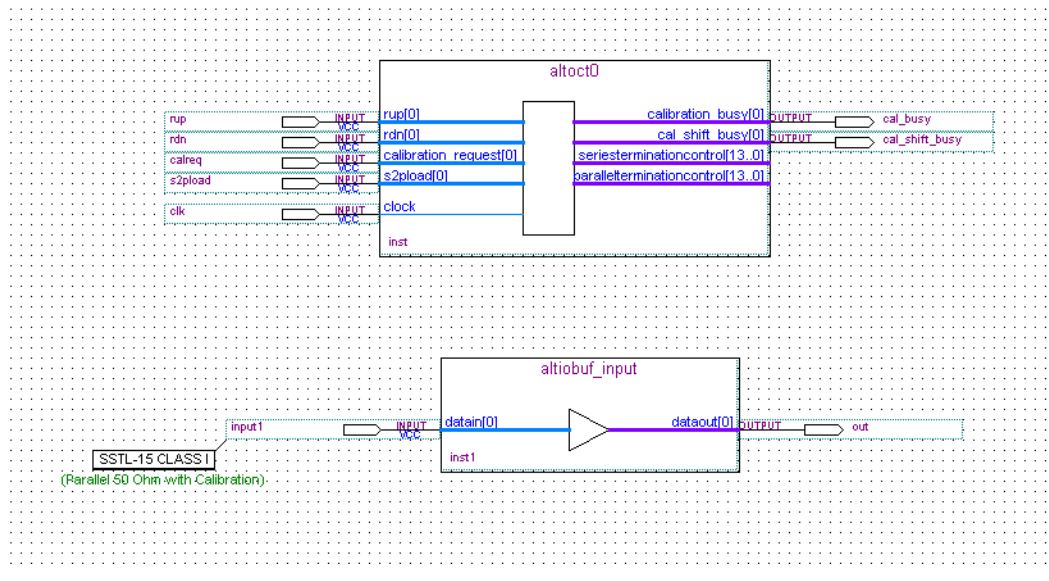
For more information about the ALTOCT megafunction and its design examples, refer to the *ALTOCT Megafunction User Guide*.

The ALTIobuf megafunction in the Quartus II software implements either an input buffer, output buffer, or an bidirectional buffer. You can use user mode calibration with the ALTIobuf megafunction to instantiate the pins that require calibrated OCT.

Example Design 1 for Input Pins

This example describes how to implement user mode calibration for input pins. [Figure 5](#) shows a schematic representation of the user mode OCT calibration design for an input pin.

Figure 5. Block Diagram: Example Design 1

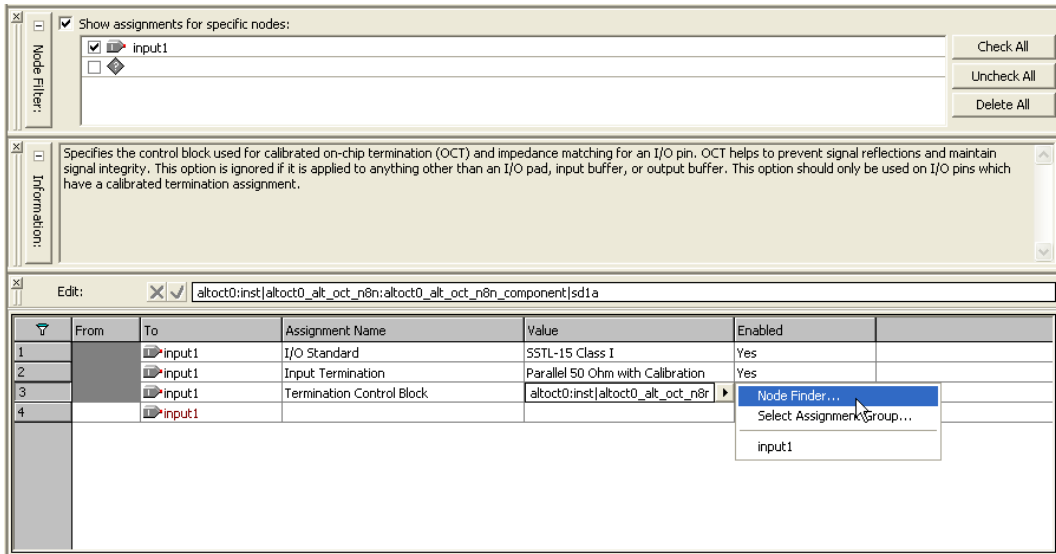


In the ALTIobuf megafunction for an input buffer (Figure 5), the signal from the external device is `datain`. The `dataout` signal connects the I/O to the core.

The following steps describe the design flow for the design:

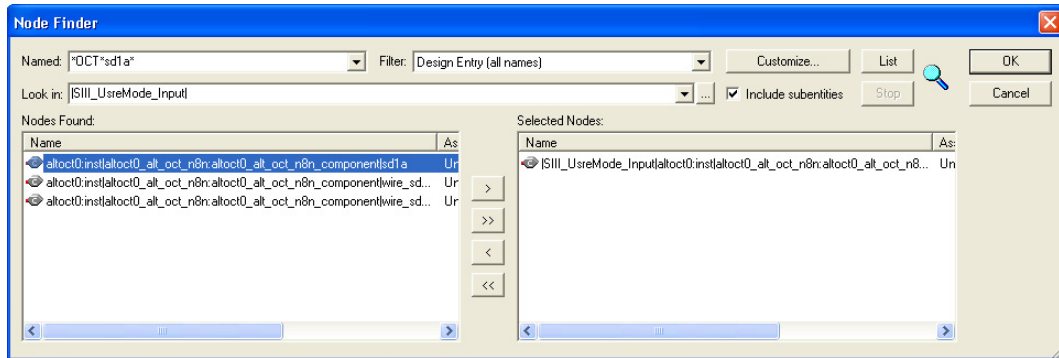
1. Instantiate the ALTOCT megafunction. The number of OCT calibration blocks required by the design is specified when instantiating the ALTOCT megafunction. One OCT calibration block is used in this example. The `seriesterminationcontrol` and `parallelerminationcontrol` signals are connected internally in the Quartus II software.
2. Instantiate the ALTIobuf megafunction for input pin associated with one I/O buffer. Input pin `input1` is shown in Figure 5.
3. On the Processing menu, point to Start and click **Start Analysis & Elaboration**.
4. Using the Assignment Editor. Assign **SSTL-15 Class I** I/O standard to the input pin `input1` (Figure 6).

Figure 6. Assignment Editor in the Quartus II Software: Example Design 1



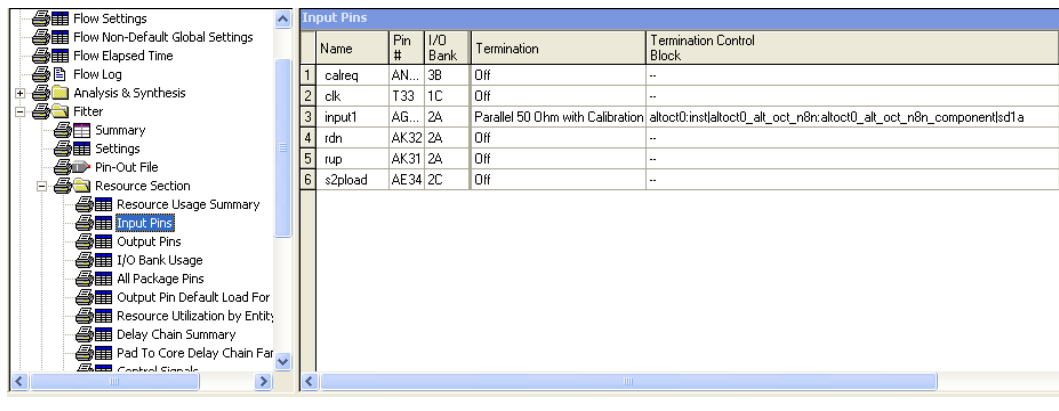
5. Assign Input Termination with **Parallel 50 Ohm with Calibration** to the input pin `input1`.
6. In the Assignment Editor, use the Termination Control Block assignment and specify the OCT calibration block instance name in the **Value** column. To get the name of the control block, double-click the **Value** field in the Assignment Editor and click **Node Finder** (Figure 6).
7. In the Node Finder, type in search expression `*OCT*sd1a*` in the **Named** box. In the Filter box, select **Design Entry** (Figure 7).

Figure 7. Node Finder in the Quartus II Software: Example Design 1



8. Click **List** to select the appropriate control block instance name for the pin under **Nodes Found** and click **OK** to make the assignment. If the design has multiple instances, then the instances are numbered `sd1a_0`, `sd1a_1`, and so on.
9. Compile the design.
10. The report file for input pins (Figure 8) shows the R_{UP} , R_{DN} , and input pins bank location for the OCT calibration block.

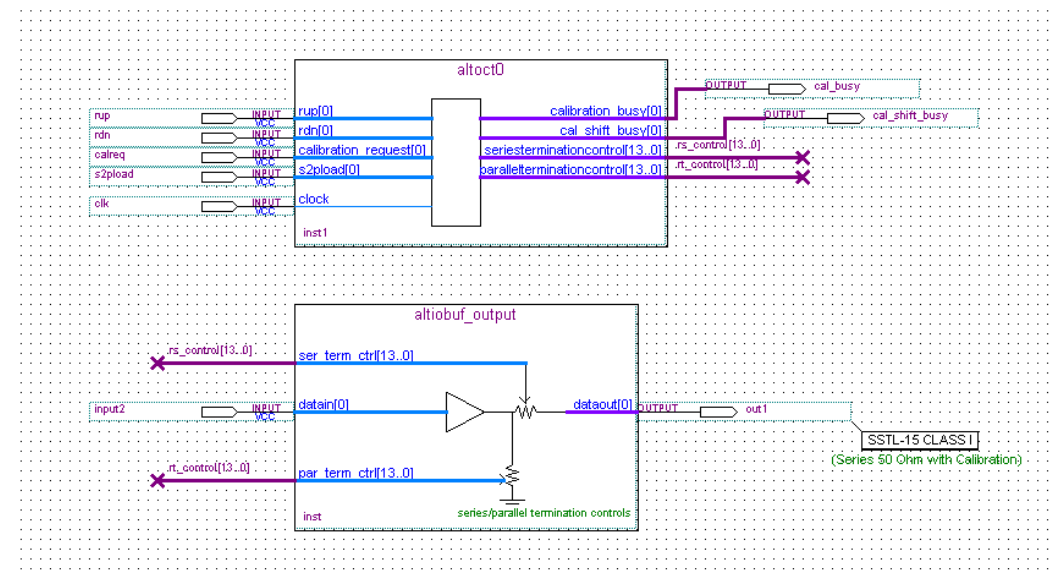
Figure 8. Compilation Report for Input Pins: Example Design 1



Example Design 2 for Output Pins

This example describes how to implement user mode calibration for output pins. Figure 9 shows a schematic representation of the user mode OCT calibration design for output pins.

Figure 9. Block Diagram: Example Design 2



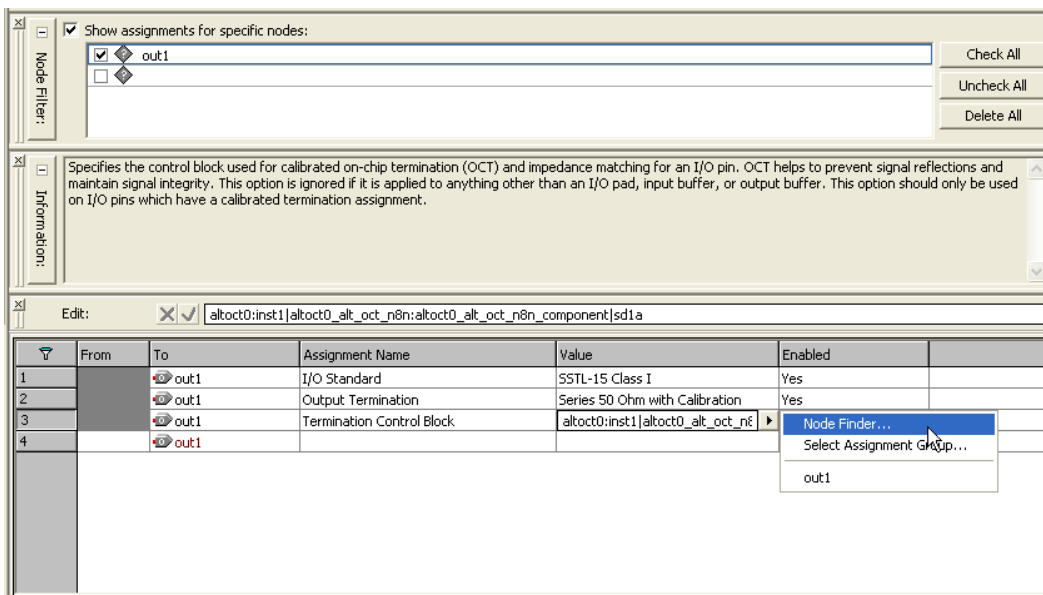
In the ALTIobuf megafunction, for an I/O output buffer (see Figure 9), the signal from the core is datain. The dataout signal connects the I/O to the external device. Each of the 14-bit ser_term_ctrl and par_term_ctrl signals are fed by the OCT calibration block.

The following steps describe the design flow for the design:

1. Instantiate the ALTOCT megafunction. The number of OCT calibration blocks required by the design is specified when instantiating the ALTOCT megafunction. One OCT calibration block is used in this example.
2. Connect the seriesterminationcontrol and parallelterminationcontrol output ports to the 14-bit rs_control and 14-bit rt_control signal bus, respectively. Because the output pins do not support OCT R_T , the 14-bit OCT R_S calibration code is placed in the 14 registers for OCT R_T calibration and the 14 registers for OCT R_S calibration.

3. Instantiate the ALTIOBUF megafunction for output pin associated with one I/O buffer. Output pin `out1` is shown in [Figure 9](#).
4. Connect the `ser_term_ctrl` and `par_term_ctrl` input ports to the 14-bits `rs_control` and 14-bits `rt_control` signal bus, respectively. Each of the 14-bit `ser_term_ctrl` and `par_term_ctrl` signals are fed by the OCT calibration block.
5. On the Processing menu, point to Start and click **Start Analysis & Elaboration**.
6. Using Assignment Editor, assign **SSTL-15 Class I** I/O standard to the output pin `out1` ([Figure 10](#)).

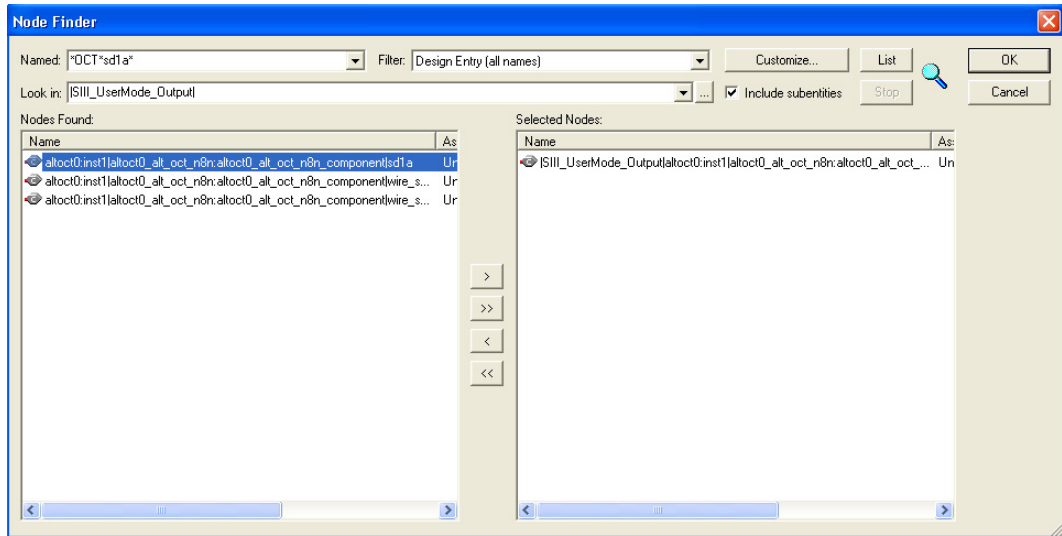
Figure 10. Assignment Editor in the Quartus II Software: Example Design 2



7. Assign the output termination with **Series 50 Ohm with Calibration** to the output pin `out1`.
8. In the Assignment Editor, use the Termination Control Block assignment and specify the OCT calibration block instance name in the **Value** column. To get the name of the control block, double-click the **Value** field in the Assignment Editor and click **Node Finder** ([Figure 10](#)).

9. In Node Finder, type *OCT*sd1a* in the **Name** box and in the Filter list, select **Design Entry** (Figure 11).

Figure 11. Node Finder in the Quartus II Software: Example Design 2



10. Click **List** to select the appropriate control block instance name for the pin under **Nodes Found** and click **OK** to make the connection. If the design has multiple instances, then the instances are numbered sd1a_0, sd1a_1, and so on.
11. Compile the design.
12. The report file for input pins (Figure 12) shows the R_{UP} and R_{DN} pins bank location for the OCT calibration block.

Figure 12. Compilation Report for Input Pins: Example Design 2

| | Name | Pin # | I/O Bank | Termination | Termination Control Block | Location assigned by |
|---|---------|-------|----------|-------------|---------------------------|----------------------|
| 1 | calreq | AH19 | 3C | Off | -- | Filter |
| 2 | clk | T33 | 1C | Off | -- | Filter |
| 3 | input2 | AE34 | 2C | Off | -- | Filter |
| 4 | rdn | AK32 | 2A | Off | -- | Filter |
| 5 | rup | AK31 | 2A | Off | -- | Filter |
| 6 | s2pload | AB29 | 2C | Off | -- | Filter |

- The report file for output pin out1 (Figure 13) shows the bank location for the OCT calibration block.

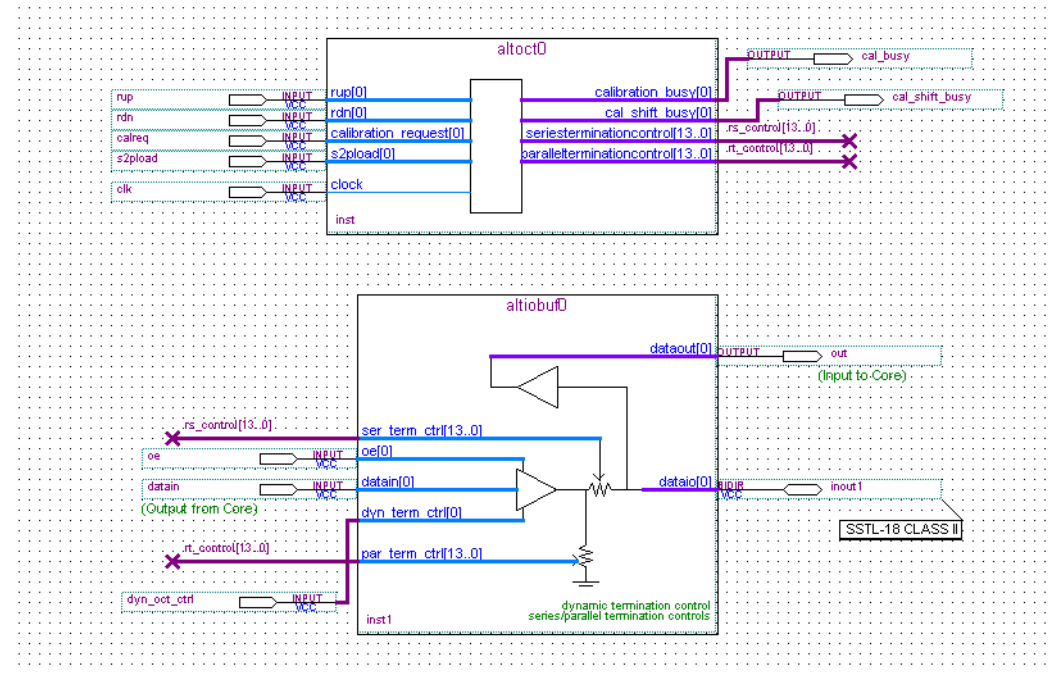
Figure 13. Compilation Report for Output Pins: Example Design 2

| | Name | Pin # | Termination | Termination Control Block |
|---|----------------|-------|-----------------------------------|---|
| 1 | cal_busy | AL18 | Series 50 Ohm without Calibration | -- |
| 2 | cal_shift_busy | AE19 | Series 50 Ohm without Calibration | -- |
| 3 | out1 | AG33 | Series 50 Ohm with Calibration | altoct0:inst1 altoct0_alt_oct_n8n:altoct0_alt_oct_n8n_component\$sd1a |

Example Design 3 for Bidirectional Pins

This example describes how to implement user mode calibration for bidirectional pins. Figure 14 shows a schematic representation of the user mode OCT calibration design for bidirectional pin.

Figure 14. Block Diagram: Example Design 3



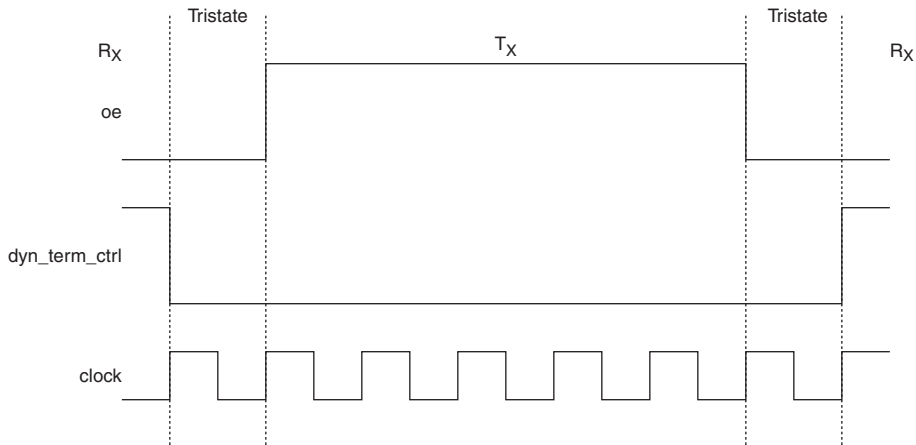
In the ALTIobuf megafunction for a bidirectional buffer (see Figure 14), signal `dataio` connects the bidirectional pin to the external device. The output signal from the core is `datain`. The input signal from the bidirectional buffer to the core is `dataout`. Each of the 14-bit `ser_term_ctrl` and `par_term_ctrl` signals are fed by the OCT calibration block. Input signals `oe` and `dyn_term_ctrl` are used to switch the bidirectional pin between input and output mode, and turn on or off dynamic R_T . Table 1 summarizes the logic level for `oe` and `dyn_term_ctrl` when the bi-directional pin is operating in either output or input mode. Signals `oe` and `dyn_term_ctrl` should be generated by user logic.

Table 1. Logic State of `oe` (Output Enable) and Dynamic Termination Control for Bi-Directional Pin in Either Input or Output Mode

| Mode | oe | dyn_term_ctrl | Dynamic R_T |
|--------|----|---------------|---------------|
| Input | 0 | 1 | On |
| Output | 1 | 0 | Off |

The dynamically terminated input signals to the bidirectional I/O buffer should have the following timing relationship (Figure 15). `dyn_term_ctrl` must be de-asserted at least one clock cycle before `oe` goes high and asserted at least one clock cycle after `oe` goes low.

Figure 15. Timing Diagram for Signals `oe` and `dyn_term_ctrl`



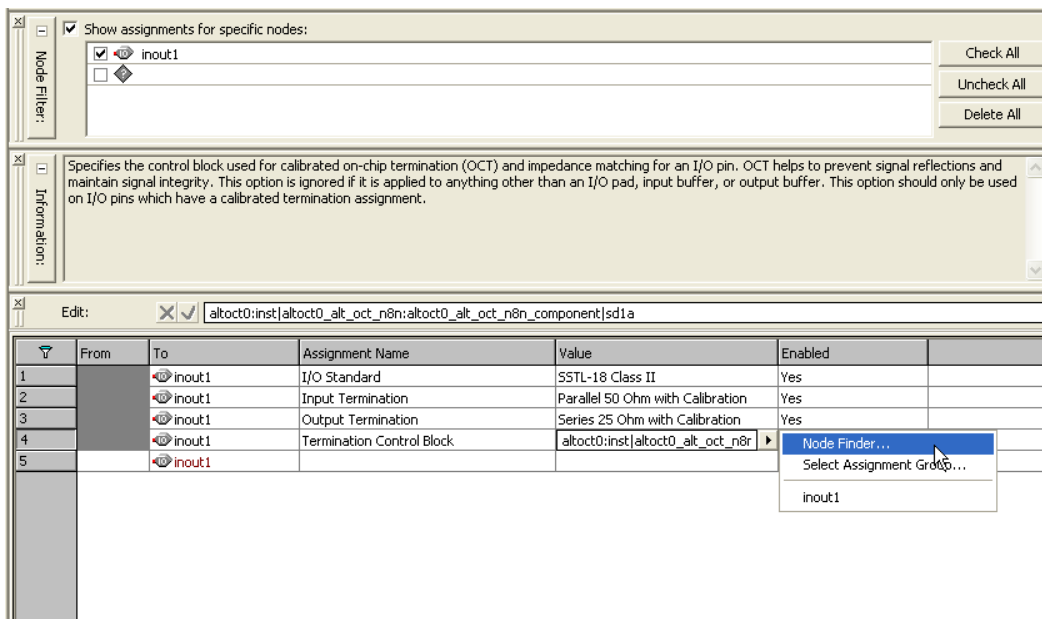
For timing specifications, refer to the *DC and Switching Characteristics of Stratix III Devices* chapter in volume 2 of the *Stratix III Device Handbook*.

The following steps describe the design flow for the design:

1. Instantiate the ALTOCT megafunction. The number of OCT calibration blocks required by the design is specified when instantiating the ALTOCT megafunction. One OCT calibration block is used in this example.
2. Connect the `seriesterminationcontrol` and `parallelerminationcontrol` output ports to the 14-bit `rs_control` and 14-bit `rt_control` signal bus, respectively.
3. Instantiate the ALTIOBUF megafunction for bidirectional pin associated with one calibration block. Bidirectional pin `inout1` is shown in [Figure 14 on page 14](#).
4. Connect the `ser_term_ctrl` and `par_term_ctrl` input ports to the 14-bit `rs_control` and 14-bit `rt_control` signal bus, respectively. Each of the 14-bit `ser_term_ctrl` and `par_term_ctrl` signals are fed by the OCT calibration block.

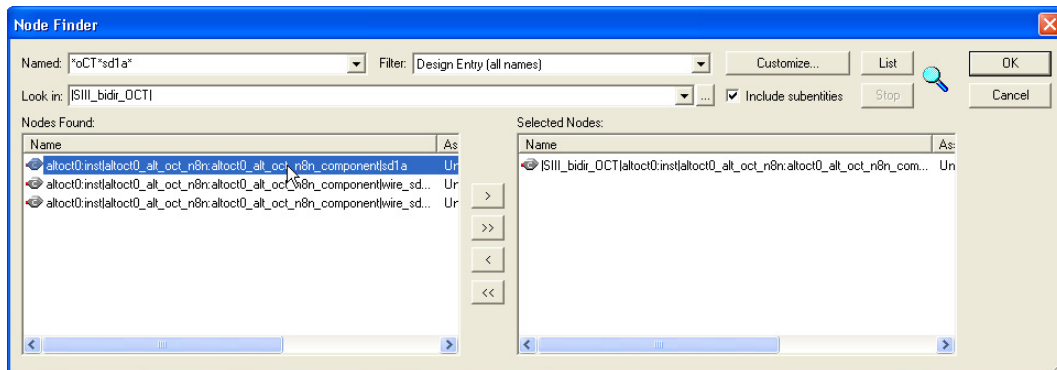
5. On the Processing menu, point to Start and click **Start Analysis & Elaboration**.
6. Using the Assignment Editor, assign **SSTL-18 Class II I/O** standard to the bidirectional pin `inout1` (Figure 16).

Figure 16. Assignment Editor in the Quartus II Software: Example Design 3



7. Assign the Input Termination assignment with **Parallel 50 Ohm with Calibration** and output termination with **Series 25 Ohm with Calibration** to the bidirectional pin `inout1`.
8. In the Assignment Editor, use the Termination Control Block assignment and specify the OCT calibration block instance name in the **Value** column. To get the name of the control block, double-click the **Value** field in the Assignment Editor and click **Node Finder** (Figure 16).
9. In Node Finder, type `*OCT*sd1a*` in the **Name** box. In the **Filter** list, select **Design Entry** (Figure 17).

Figure 17. Node Finder in the Quartus II Software: Example Design 3



10. Click **List** to select the appropriate control block instance name for the pin under **Nodes Found** and click **OK** to make the assignment. If the design has multiple instances, then the instances are numbered `sd1a_0`, `sd1a_1`, and so on.
11. Compile the design.
12. The report file for input pins (Figure 18) shows the R_{UP} and R_{DN} pins bank location for the OCT calibration block.

Figure 18. Compilation Report for Input Pins: Example Design 3

| Input Pins | | | | | | | |
|------------|--------------|-------|----------|-------------|---------------------------|----------------------|--|
| | Name | Pin # | I/O Bank | Termination | Termination Control Block | Location assigned by | |
| 1 | calreq | AA29 | 2C | Off | .. | Filter | |
| 2 | clk | T33 | 1C | Off | .. | Filter | |
| 3 | dainain | AC31 | 2C | Off | .. | Filter | |
| 4 | dyn_oct_ctrl | AE34 | 2C | Off | .. | Filter | |
| 5 | oe | AB29 | 2C | Off | .. | Filter | |
| 6 | rdn | AK32 | 2A | Off | .. | Filter | |
| 7 | rup | AK31 | 2A | Off | .. | Filter | |
| 8 | s2pload | AB30 | 2C | Off | .. | Filter | |

13. The report file for bidirectional pin `inout1` (Figure 19) shows the bank location for the OCT calibration block.

Figure 19. Compilation Report for Bidirectional Pins: Example Design 3

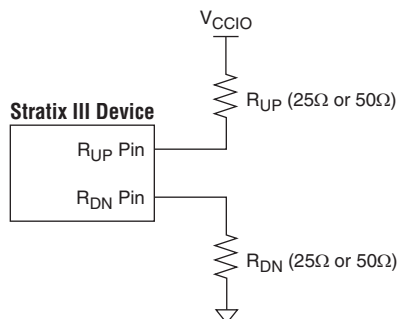
| Name | Pin # | I/O Bank | I/O Standard | Input Termination | Output Termination | Termination Control Block | |
|------|--------|----------|--------------|-------------------|----------------------------------|--------------------------------|--|
| 1 | inout1 | AG33 | 2A | SSTL-18 Class II | Parallel 50 Ohm with Calibration | Series 25 Ohm with Calibration | altoct0:inst1altoct0_alt_oct_n8n:altoct0_alt_oct_n8n_compone |

Design Considerations When Using OCT Calibration

You must follow the information in this section when you use OCT calibration:

- Place R_{UP} and R_{DN} resistors on the board. Each calibration block has one pair of R_{UP} and R_{DN} pins associated with it. These pins can be connected to 50 Ω or 25 Ω external reference resistors. The same calibration block can drive multiple pins if they have the same termination values and the same V_{CCIO} . The R_{UP} and R_{DN} pins determine whether you are trying to achieve 50 Ω or 25 Ω OCT resistance. The calibration circuit in Stratix III devices relies on R_{UP} and R_{DN} for accurate on-chip series and parallel termination.

Connect the R_{UP} pin to V_{CCIO} of the bank in which the calibration block resides through an external 25 Ω or 50 Ω resistor (as shown in Figure 20). Connect the R_{DN} pin to ground through an external 25 Ω or 50 Ω resistor. Both R_{UP} and R_{DN} are required for correct operation and must be the same value. For parallel (R_T) OCT, use 50 Ω external resistors for R_{UP} and R_{DN} .

Figure 20. External R_{UP} and R_{DN} Connections on a PCB

- Use 1% discrete resistors for R_{UP} and R_{DN} .
- Use wide and short traces for R_{UP} and R_{DN} resistor connections on the board.
- A bidirectional pin that uses both 25Ω/50Ω (output) and 50Ω (input) termination values should connect to a calibration block that uses 50-Ω external reference resistors. The 25-Ω termination on the bidirectional pin is achieved through internal divide by two circuit.
- The I/O pin should be connected to, or associated with, an OCT calibration block with the same V_{CCIO} as the I/O pin.
- Only one instance of the ALTOCT megafunction is allowed in the design. You can specify the number of OCT calibration blocks in the design using the ALTOCT MegaWizard Plug-In Manager.
- Only one calibration block can drive an I/O bank.
- Stratix III devices do not support multiply circuitry to achieve 50Ω termination on the bidirectional pin using 25Ω R_{UP} and R_{DN} external resistors.

Design Examples Download

The following links provide the design examples:

- [Design Example 1 \(SIII_UserMode_Input.qar\)](#)
- [Design Example 2 \(SIII_UserMode_Output.qar\)](#)
- [Design Example 3 \(SIII_bidir_OCT.qar\)](#)
- [Stratix III OCT Power Up Example \(SIII_OCT_Powerup_Example.qar\)](#)

Conclusion

Stratix III devices supports power-up mode or user mode OCT calibration for optimal termination value. This application note discusses the use of the OCT calibration block with input, output, and bidirectional pins for Stratix III devices using the Quartus II software version 7.2 or later.

Revision History

Table 2 shows the revision history for this application note.

| <i>Table 2. Revision History</i> | | |
|----------------------------------|---------------------|-----------------|
| Date and Version | Changes Made | Comments |
| December 2007, v1.0 | Initial release. | — |