

Introduction

The Stratix® IV family of devices from Altera is based on 0.9 V, 40 nm Process technology. Stratix IV FPGAs deliver a high level of performance and power efficiency for high-end applications. The innovative architecture of Stratix IV devices is optimized to get the maximum power saving through a variety of process, circuit, and architecture optimizations and innovations. The advanced architecture of Stratix IV devices features triple-gate oxide, all-copper routing with low-k dielectric material that dramatically reduces power and improves performance. Stratix IV devices include advanced, efficient logic structures called adaptive logic modules (ALMs) that obtain maximum performance while minimizing power consumption.

Altera provides the Quartus® II PowerPlay Power Analyzer tool to aid you during the design process by delivering fast and accurate estimations of power consumption. You can use this information to locate the blocks in your design that are consuming the most power and target those blocks to minimize the power consumption of your design.



For more information about the PowerPlay Power Analyzer, refer to the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Designing for Low Power

Total FPGA power consumption consists of I/O power, core static power, and core dynamic power. This application note focuses on design optimization options and techniques that help reduce core dynamic and core static power in Stratix IV devices. These techniques include:

- Programmable Power Technology
- Device Selection Considerations

This application note describes these power optimization techniques in detail and provides information about how to use them effectively.



For more information about low power design techniques that can further reduce your design power usage by implementing changes at the design level, refer to the *Power Optimization* chapter in volume 2 of the *Quartus II Handbook*.

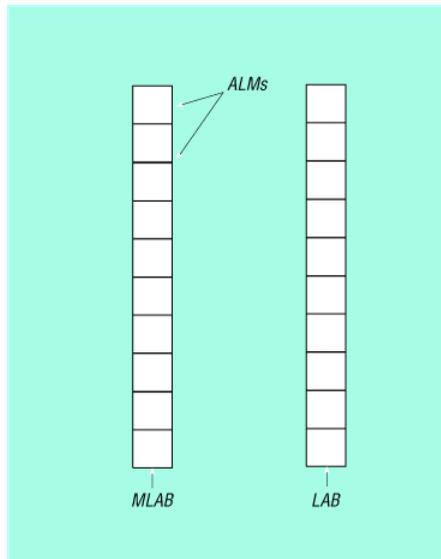
Programmable Power Technology

Programmable Power Technology enables Stratix IV core logic to be programmed at the tile level for high-speed mode or low-power mode configuration. Tiles are defined as:

- A combination of a LAB and MLAB pair (including the adjacent routing associated with LAB and MLAB, as shown in [Figure 1](#))
- A DSP block
- A memory block

Tiles can be configured to operate in high-speed mode or low-power mode.

Figure 1. Programmable Power Technology Tile View



Tiles that are in the critical timing path of a design are configured in high-speed mode to meet the timing requirements. The remaining tiles are configured in low-power mode. A small percentage of the circuit uses the high-speed mode tiles. The remaining tiles are configured as low-power mode, resulting in a significant decrease in static power for low-power mode logic.



External memory interface circuitry, PLLs, and the SERDES/DPA blocks cannot be configured in low-power mode. Memory and DSP blocks are configured in low-power mode only when they are unused.

The Quartus II software automatically controls which tiles operate in high-speed mode and which operate in low-power mode based on the timing constraint specified for the design. The **PowerPlay power optimization** option available in the **Fitter Settings** dialog box (Figure 2) controls the configuration of tiles in the high-speed mode or low-power mode, along with other power optimization techniques implemented at the Fitter level. You must provide realistic timing constraints for your design to achieve the lowest possible power consumption. After meeting your design performance goal, the Fitter employs extra effort to reduce the power consumption of your design, if you direct it to do so.

Figure 2. Fitter Settings Dialog Box

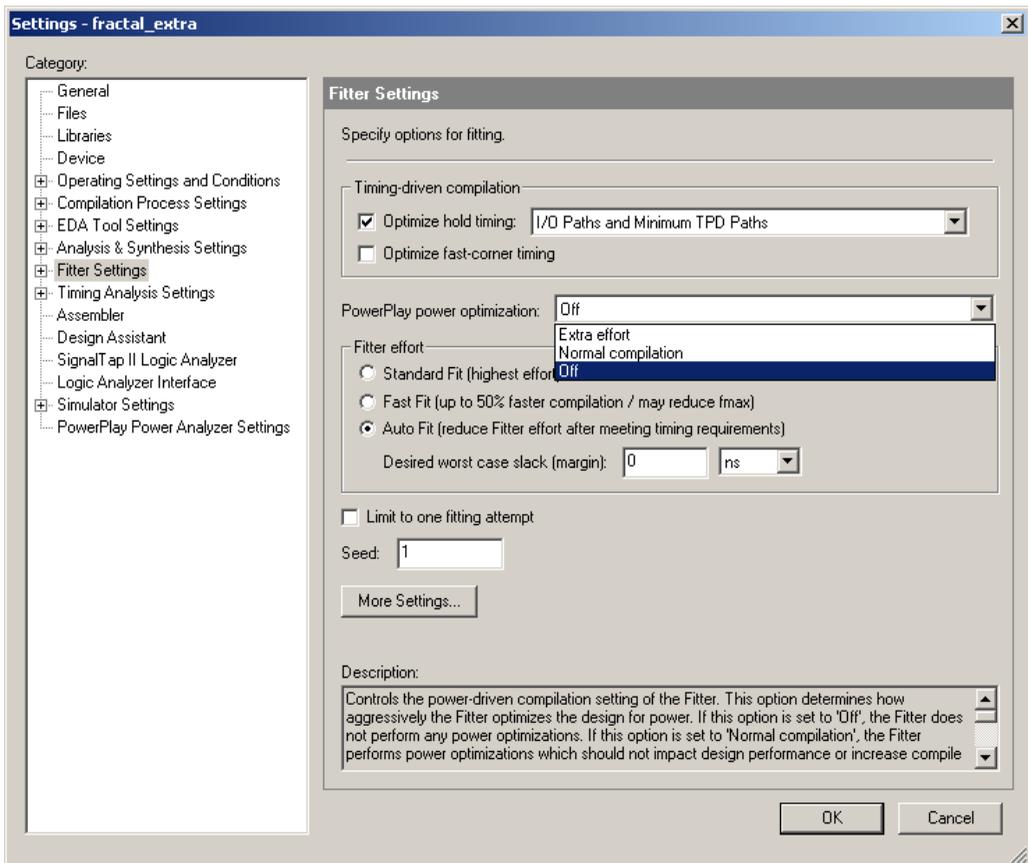


Table 1 lists the settings for the **PowerPlay power optimization** option. These settings can only be applied on a project-wide basis. The **Extra effort** setting requires the Fitter to employ extensive effort to optimize the design for power, and can increase the compilation time.

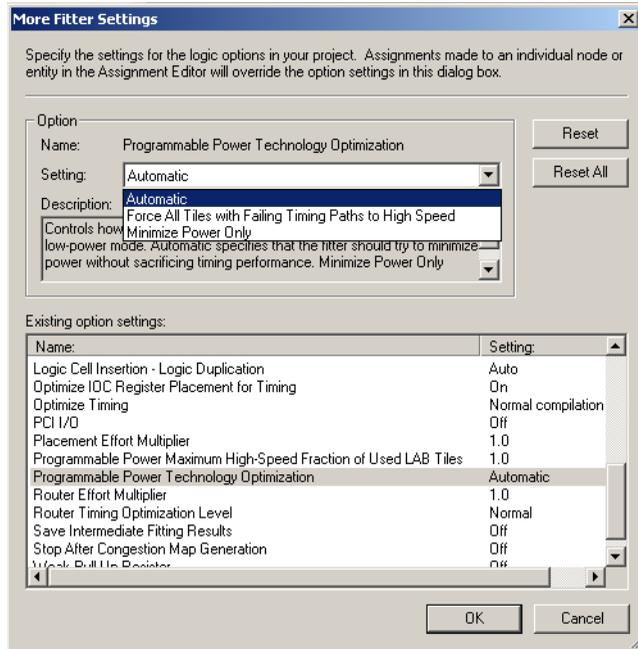
Setting	Description
Extra effort	High computing effort algorithms are applied to minimize power through placement and routing optimizations. Maximum performance might be impacted.
Normal compilation (Default)	Low computing effort algorithms are applied to minimize power through placement and routing optimizations as long as they are not expected to reduce design performance.
Off	No netlist, placement, or routing optimizations are performed to minimize power.

The **Normal compilation** setting is selected by default, and configures each tile in high-speed mode or low-power mode based on the timing constraints entered for the design. The design's critical paths are identified and the tiles along those critical paths are configured as high-speed mode tiles to meet the timing constraints. The remaining tiles are configured in low-power mode to reduce the overall design power usage.

The **Extra effort** setting performs the functions of the **Normal compilation** setting and other place-and-route optimizations during fitting to fully optimize the design for power. The Fitter applies extra effort to minimize power, even after timing requirements have been met, by effectively moving the logic closer during placement to localize high-toggling nets and using routes with low capacitance. It also looks for opportunities to configure more high-speed mode tiles into low-power mode tiles to reduce power consumption. However, this extra effort can increase the compilation time.

Another way to control the high-speed mode or low-power mode tile configuration is to enable the **Programmable Power Technology Optimization** and **Programmable Power Maximum High-Speed Fraction of Used LAB Tiles** options, available in the **Existing option settings** box in the **More Fitter Settings** dialog box, as shown in [Figure 3](#).

Figure 3. Programmable Power Technology Optimization Settings



The available settings for the **Programmable Power Technology Optimization** option are **Automatic**, **Force All Tiles with Failing Timing Paths to High Speed**, and **Minimize Power Only**. **Automatic** is the default setting, and specifies that the Fitter use the power-driven Fitter option, as described in [Table 1](#). The **Force All Tiles with Failing Timing Paths to High Speed** setting sets all tiles with failing timing paths to high speed. The default setting, which is **Automatic**, can result in some of the paths in your design not meeting timing by setting tiles to low power if these failing paths do not affect the speed of any clocks in your design. The **Force All Tiles with Failing Timing Paths to High Speed** setting sets all tiles with failing timing paths to high speed, and is useful during timing closure.

The **Minimize Power Only** setting specifies that the Fitter should set the maximum number of tiles to operate in low-power mode. This setting may impact design performance, but results in the largest power savings.

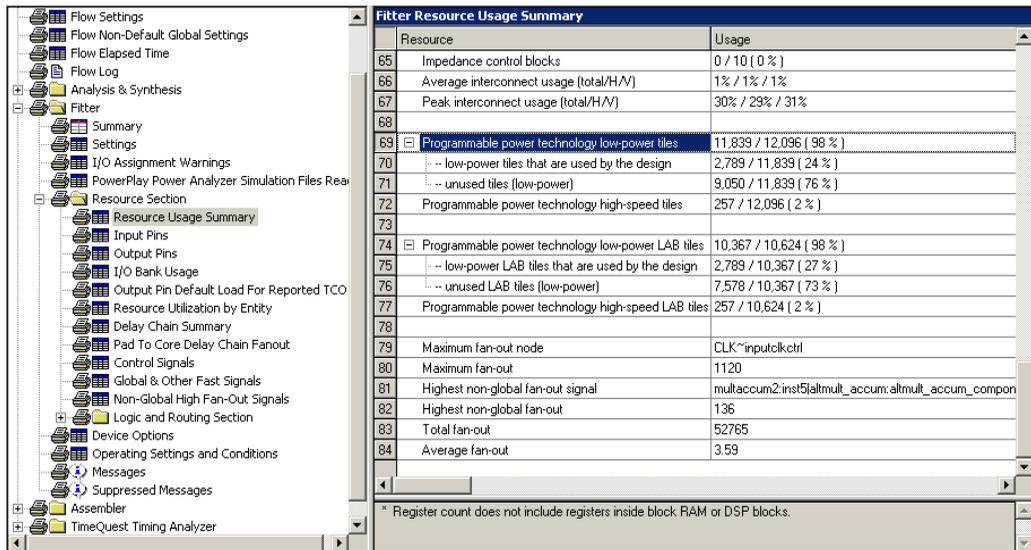
The default setting for the **Programmable Power Maximum High-Speed Fraction of Used LAB Tiles** option is 1.0. This option sets a limit on the number of high-speed tiles that can be used for your design. With the value set at 1.0, there is no restriction on the number of high-speed tiles,

and the Fitter uses the minimum number needed to meet the timing requirements of your design. Specifying a value lower than 1.0 may degrade timing quality, because some timing critical resources might be forced into low-power mode.

Fitter Reports

The Fitter report section of the **Compilation Report** provides detailed information about the number of low-power mode tiles and LAB tiles used in the design. The **Fitter Resource Usage Summary** shows the Programmable Power Technology low-power tiles, Programmable Power Technology high-speed tiles, Programmable Power Technology low-power LAB tiles, and Programmable Power Technology high-speed LAB tiles usage information for Stratix IV devices (Figure 4). This information is further divided into actual low-power mode tiles and LAB tiles used by the design, as well as unused tiles and LAB tiles that are automatically configured in low-power mode by the Quartus II software.

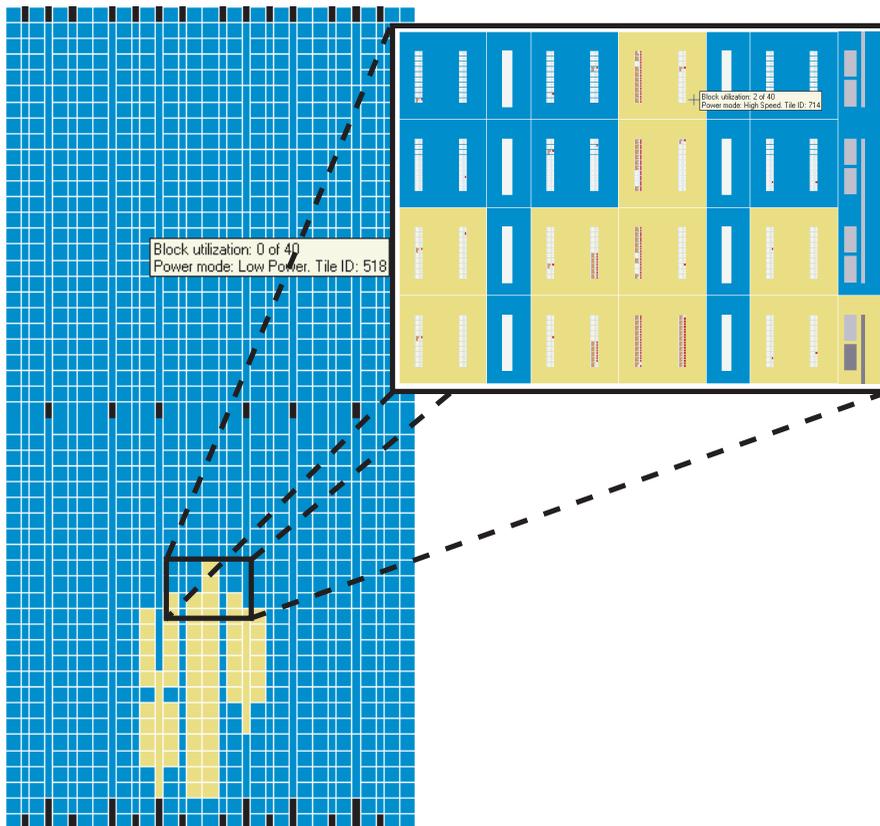
Figure 4. Fitter Resource Usage Summary



Chip Planner View

The Chip Planner tool in the Quartus II software enables you to view high-speed mode and low-power mode tiles implemented for your Stratix IV design. To start the Chip Planner, on the Tools menu, click **Chip Planner (Floorplan and Chip Editor)**. The **Power Analysis (Assignment)** mode view setting under the **Layer set** option provides a hierarchical view of your design implementation. This view shows the high-speed mode and low-power mode tiles used for your design in different colors to make it easier to distinguish between them (Figure 5).

Figure 5. Chip Planner View with Power Analysis (Assignment) Mode



When you place the cursor over a resource at this level, a tooltip appears that describes the power mode for that particular tile. The Chip Planner also enables you to view the internal structure of Altera® devices and incrementally edit logic element (LE) and I/O cell configuration after place-and-route has been performed.



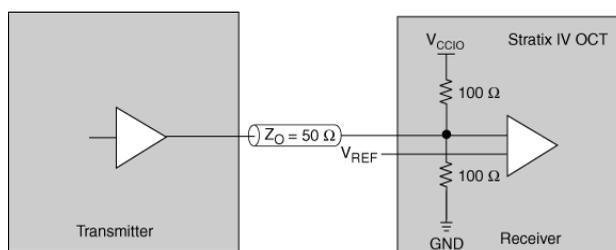
For more information about the Chip Planner tool, refer to the *Engineering Change Management with the Chip Planner* chapter in volume 2 of the *Quartus II Handbook*.

Dynamically-Controlled On-Chip Terminations

Stratix IV FPGAs offer dynamic on-chip termination (OCT). Dynamic OCT enables series termination (RS) and parallel termination (RT) to dynamically turn on or off during the data transfer. This feature is especially useful when Stratix IV FPGAs are used with external memory interfaces, such as interfacing with DDR memories.

Compared to conventional termination, dynamic OCT reduces power consumption significantly because it eliminates the constant DC power consumed by parallel termination when transmitting data. Parallel termination is extremely useful for applications that interface with external memories where I/O standards, such as HSTL and SSTL, are used. Parallel termination supports dynamic OCT, which is useful for bidirectional interfaces (Figure 6).

Figure 6. Stratix IV On-Chip Parallel Termination



The following is an example of power saving for a DDR3 interface using on-chip parallel termination.

The static current consumed by parallel OCT is equal to the V_{CCIO} voltage divided by $100\ \Omega$. For a DDR3 interface that uses SSTL-15, the static current is $1.5\ \text{V}/100\ \Omega = 15\ \text{mA}$ per pin. Therefore, the static power is $1.5\ \text{V} * 15\ \text{mA} = 22.5\ \text{mW}$. For an interface with 72 DQ and 18 DQS pins, the static power is $90\ \text{pins} * 22.5\ \text{mW} = 2.025\ \text{W}$. Dynamic parallel OCT disables parallel termination only during write operations; therefore, if writing occurs 50% of the time, the power saved by dynamic parallel OCT is $50\% * 2.025\ \text{W} = 1.0125\ \text{W}$.



For more information about dynamic OCT in Stratix IV devices, refer to the *Stratix IV Device I/O Features* chapter in the *Stratix IV Device Handbook*.

Device Selection Considerations

Different device families have different power characteristics. Many parameters affect a device family's power consumption, including choice of process technology, supply voltage, electrical design, and device architecture. In addition to these parameters, power in the Stratix IV family of devices is also affected by the speed grade selection. Speed grades describe the relative speed of each device. The lower the number, the faster the device. For example, the -2 speed grade device is the fastest, the -3 speed grade device is medium speed, and the -4 speed grade device is the slowest. For Stratix IV devices, choosing a faster speed grade device can lead to increased performance and reduced static power for your design. This level of power saving is achieved by using the Programmable Power Technology, which reduces the number of high-speed mode tiles needed to meet timing in the faster speed grade device.

Faster speed grade devices may be beneficial in a variety of situations. For example, if you compile your design in a medium speed grade Stratix IV device and meet your performance goal with 20% utilization of high-speed tiles, you can further reduce the power consumption of your design by selecting a faster speed grade device. The faster speed grade device allows you to meet your performance requirement and use fewer high-speed mode tiles than the medium speed grade device, reducing the total power consumption of your design.



If you meet your performance and power requirements by selecting a low operating voltage for your selected Stratix IV device, there is no need to move to a faster speed grade device. However, if the absolute lowest power is required, move to a faster speed grade device, which will result in higher performance and the lowest possible power consumption.

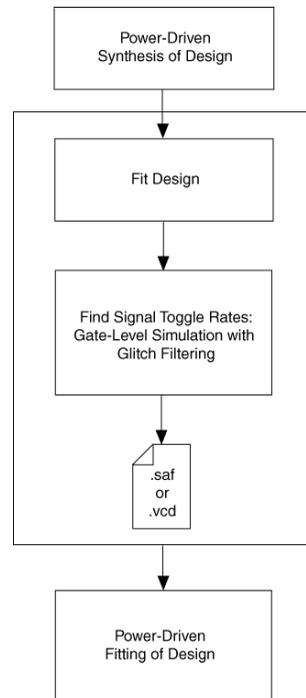


For more information about device selection considerations, refer to the *PowerPlay Power Analysis* chapter in volume 2 of the *Quartus II Handbook*.

Quartus II PowerPlay Power Optimization Flow

The recommended design flow to fully optimize a design for power during compilation using the Quartus II software is shown in [Figure 7](#). This flow uses the power-driven compilation options available in the Quartus II software.

Figure 7. Recommended Design Flow for Power-Driven Compilation



The power-driven compilation takes place at the synthesis and Fitter levels. Power-driven synthesis changes the synthesis netlist to optimize the design for power. Power-driven synthesis settings perform memory optimization and power-aware logic mapping during synthesis. The power-driven Fitter (**Extra effort** setting) performs place-and-route optimization and controls the high-speed mode or low-power mode tiles configuration during fitting to fully optimize the design for power, as described in the “[Programmable Power Technology](#)” section.



For more information about power-driven compilation and low-power design techniques, refer to the [Power Optimization](#) chapter in volume 2 of the *Quartus II Handbook*.

Accurate toggle-rate data information about each signal in your design is important for optimizing design power during place-and-route. The power-driven Fitter uses this information to guide the Fitter and optimize the design power based on the signal activity information of the design. The most accurate signal activity provides the best power optimization during fitting. Signal activities from full, post-fit netlist (timing) simulation provide the highest accuracy, because all node activities reflect actual design behavior, if supplied input vectors are representative of typical design operation. To use the signal activities information from post-fit simulation, you must compile the design using the default settings (**Normal compilation**). Simulate your design using gate-level simulation and generate a signal activity file (.saf or .vcd) for the design. Recompile the design using the power-driven fitting (**Extra effort**) that uses the design signal activities information to further optimize the design for power, as shown in [Figure 7](#). This procedure makes the design flow a bit more time-consuming but is very effective for design power optimization.



For more information about how to create a signal activities file (.saf or .vcd), refer to the [PowerPlay Power Analysis](#) chapter in volume 3 of the *Quartus II Handbook*.

Conclusion

Historically, performance has been the main criterion in selecting an FPGA. With the introduction of the latest 40 nm technology, power consumption is fast becoming a critical selection criterion. To accommodate this newly introduced design constraint, Stratix IV devices are designed to allow low power consumption without compromising performance. Innovative architecture and Programmable Power Technology options provide the best combination to offer designers the choice of performance circuitry versus low-power mode circuitry.

Referenced Documents

This application note references the following documents:

- [Engineering Change Management with the Chip Planner](#) chapter in volume 2 of the *Quartus II Handbook*
- [Power Optimization](#) chapter in volume 2 of the *Quartus II Handbook*
- [PowerPlay Power Analysis](#) chapter in volume 3 of the *Quartus II Handbook*
- [Stratix IV Device I/O Features](#) chapter in the *Stratix IV Device Handbook*

Document Revision History

Table 2 shows the revision history for this application note.

Date and Document Version	Changes Made	Summary of Changes
May 2008, v1.0	Initial release	—



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