

AN 522: Implementing Bus LVDS Interface in Supported Intel® FPGA Device Families



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Implementing Bus LVDS Interface in Supported Intel® FPGA Device Families

Bus LVDS (BLVDS) extends the capability of LVDS point-to-point communication to multipoint configuration. Multipoint BLVDS offers an efficient solution for multipoint backplane applications.

Table 1. BLVDS Implementation Support in Intel FPGA Devices

You can implement BLVDS interfaces in these Intel devices using the listed I/O standards.

Series	Family	I/O Standard
Stratix®	Stratix V	<ul style="list-style-type: none"> Differential SSTL-2 Class I Differential SSTL-2 Class II
	Stratix IV	
	Stratix III	
Arria®	Intel Arria 10	<ul style="list-style-type: none"> Differential SSTL-18 Class I Differential SSTL-18 Class II
	Arria V	<ul style="list-style-type: none"> Differential SSTL-2 Class I Differential SSTL-2 Class II
	Arria II	
Cyclone®	Intel Cyclone 10 GX	<ul style="list-style-type: none"> Differential SSTL-18 Class I Differential SSTL-18 Class II
	Intel Cyclone 10 LP	BLVDS
	Cyclone V	<ul style="list-style-type: none"> Differential SSTL-2 Class I Differential SSTL-2 Class II
	Cyclone IV	BLVDS
	Cyclone III LS	
	Cyclone III	
MAX®	Intel MAX 10	BLVDS

Note: The programmable drive strength and slew rate features in these devices allow you to customize your multipoint system for maximum performance. To determine the maximum data rate supported, perform a simulation or measurement based on your specific system setup and application.

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[BLVDS Design Example](#) on page 10

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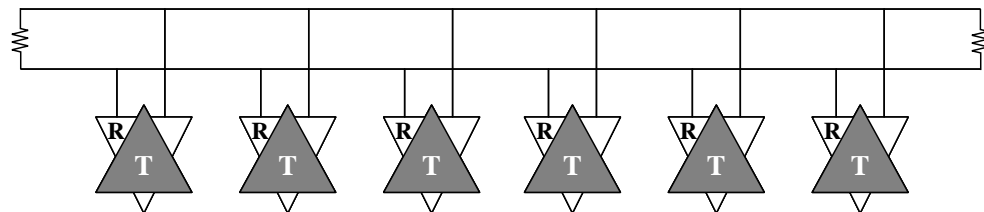
Related Links

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BLVDS Overview

Typical multipoint BLVDS system consists of a number of transmitter and receiver pairs (transceivers) that are connected to the bus.

Figure 1. Multipoint BLVDS



The configuration in the preceding figure provides bidirectional half-duplex communication while minimizing interconnect density. Any transceiver can assume the role of a transmitter, with the remaining transceivers acting as receivers (only one transmitter can be active at a time). Bus traffic control, either through a protocol or hardware solution is typically required to avoid driver contention on the bus. The performance of a multipoint BLVDS is greatly affected by the capacitive loading and termination on the bus.

Design Considerations

A good multipoint design must consider the capacitive load and termination on the bus to obtain better signal integrity. You can minimize the load capacitance by selecting a transceiver with low pin capacitance, connector with low capacitance, and keeping the stub length short.

One of the multipoint BLVDS design consideration is the effective differential impedance of a fully loaded bus, referred to as effective impedance, and the propagation delay through the bus.

Other multipoint BLVDS design considerations include fail-safe biasing, connector type and pin-out, PCB bus trace layout, and driver edge rate specifications.

Effective Impedance

The effective impedance depends on the bus trace characteristic impedance Z_0 and capacitive loading on the bus. The connectors, the stub on the plug-in card, the packaging, and the receiver input capacitance all contribute to capacitive loading, which reduces the bus effective impedance.



Equation 1. Effective Differential Impedance Equation

Use this equation to approximate the effective differential impedance of the loaded bus (Z_{eff}).

$$Z_{eff} = Z_{diff} \times \sqrt{\frac{C_o}{C_o + \frac{NC_L}{H}}} = Z_{diff} \times \sqrt{\frac{C_o}{C_o + C_d}}$$

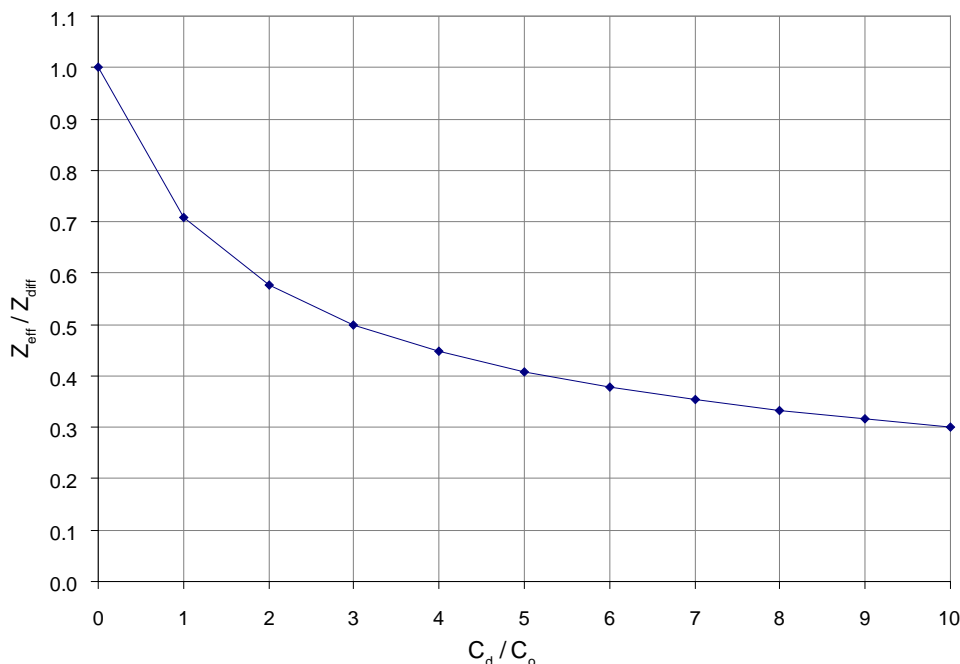
Where:

- Z_{diff} (Ω) $\approx 2 \times Z_o$ = the differential characteristic impedance of the bus
- C_o (pF/inch) = characteristic capacitance per unit length of the bus
- C_L (pF) = capacitance of each load
- N = number of loads on the bus
- H (inch) = $d \times N$ = total length of the bus
- d (inch) = spacing between each plug-in card
- C_d (pF/inch) = C_L/d = distributed capacitance per unit length across the bus

The increment in load capacitance or closer spacing between the plug-in cards reduces the effective impedance. To optimize the system performance, it is important to select a low capacitance transceiver and connector. Keep each receiver stub length between the connector and transceiver I/O pin as short as possible.

Figure 2. Normalized Effective Impedance Versus C_d/C_o

This figure shows the effects of distributed capacitance on normalized effective impedance.



Termination is required at each end of the bus, while the data flows in both directions. To reduce reflection and ringing on the bus, you must match the termination resistor to the effective impedance. For a system with $C_d/C_o = 3$, the effective impedance is 0.5 times of Z_{diff} . With double terminations on the bus, the driver sees an equivalent load of 0.25 times of Z_{diff} ; and thus reduces the signals swing and differential noise margin across the receiver inputs (if standard LVDS driver is used). The BLVDS driver addresses this issue by increasing the drive current to achieve similar voltage swing at the receiver inputs.

Propagation Delay

The propagation delay ($t_{PD} = Z_o \times C_o$) is the time delay through the transmission line per unit length. It depends on the characteristic impedance and characteristic capacitance of the bus.

Figure 3. Effective Propagation Delay

For a loaded bus, you can calculate the effective propagation delay with this equation. You can calculate the time for the signal to propagate from driver A to receiver B as the $t_{PDEFF} \times$ length of line between driver A and receiver B.

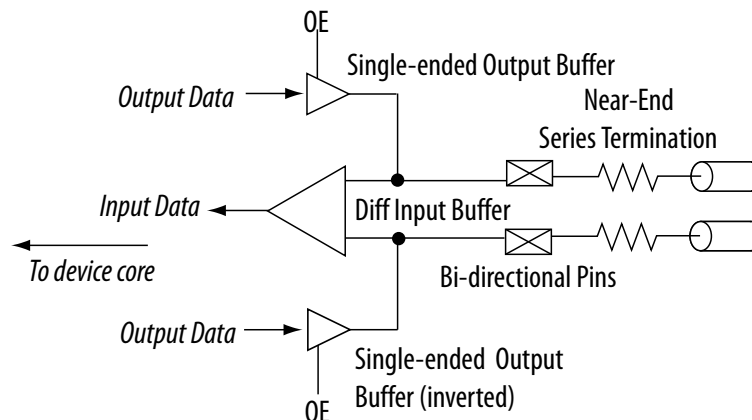
$$t_{PDEFF} = t_{PD} \times \sqrt{1 + \frac{C_d}{C_o}}$$

BLVDS Technology in Intel Devices

In supported Intel devices, the BLVDS interface is supported in any row or column I/O banks that are powered by a V_{CCIO} of 1.8 V (Intel Arria 10 and Intel Cyclone 10 GX devices) or 2.5 V (other supported devices). In these I/O banks, the interface is supported on the differential I/O pins but not on the dedicated clock input or clock output pins. However, in Intel Arria 10 and Intel Cyclone 10 GX devices, the BLVDS interface is supported on dedicated clock pins that are used as general I/Os.

- The BLVDS transmitter uses two single-ended output buffers with the second output buffer programmed as inverted.
- The BLVDS receiver uses a dedicated LVDS input buffer.

Figure 4. BLVDS I/O Buffers in the Supported Devices





Use different input or output buffers depending on the application type:

- Multidrop application—use the input or output buffer depending on whether the device is intended for driver or receiver operation.
- Multipoint application—the output buffer and input buffer shares the same I/O pins. You require an output enable (o_E) signal to tri-state the LVDS output buffer when it is not sending signals.
 - Do not enable the on-chip series termination (R_S OCT) for the output buffer.
 - Use external resistors at the output buffers to provide impedance matching to the stub on the plug-in card.
 - Do not enable the on-chip differential termination (R_D OCT) for the differential input buffer because the bus termination is usually implemented using the external termination resistors at both ends of the bus.

I/O Standards for BLVDS Interface in Intel FPGA Devices

You can implement the BLVDS interface using the relevant I/O standards and current strength requirements for the supported Intel devices.

Table 2. I/O Standard and Features Support for the BLVDS Interface in Supported Intel Devices

Devices	Pin	I/O Standard	V_{CCIO} (V)	Current Strength Option		Slew Rate	
				Column I/O	Row I/O	Option Setting	Intel Quartus Prime Setting
Intel Cyclone 10 LP Cyclone IV Cyclone III	DIFFIO	BLVDS	2.5	8, 12 (default), 16	8, 12 (default), 16	Slow	0
						Medium	1
						Fast (default)	2
Stratix IV Stratix III Arria II	DIFFIO_RX ⁽¹⁾	Differential SSTL-2 Class I	2.5	8, 10, 12	8, 12	Slow	0
						Medium	1
						Medium fast	2
						Fast (default)	3
		Differential SSTL-2 Class II	2.5	16	16	Slow	0
						Medium	1
						Medium fast	2
						Fast (default)	3
Stratix V Arria V	DIFFIO_RX ⁽¹⁾	Differential SSTL-2 Class I	2.5	8, 10, 12	8, 12	Slow	0

continued...

(1) DIFFIO_TX pin does not support true LVDS differential receivers.



Devices	Pin	I/O Standard	V _{CCIO} (V)	Current Strength Option		Slew Rate	
				Column I/O	Row I/O	Option Setting	Intel Quartus Prime Setting
Cyclone V		Differential SSTL-2 Class II	2.5	16	16	Fast (default)	1
Intel Arria 10 Intel Cyclone 10 GX	LVDS	Differential SSTL-18 Class I	1.8	4, 6, 8, 10, 12	—	Slow	0
		Differential SSTL-18 Class II	1.8	16	—	Fast (default)	1
Intel MAX 10	DIFFIO_RX	BLVDS	2.5	8, 12, 16 (default)	8, 12, 16 (default)	Slow	0
						Medium	1
						Fast (default)	2

For more information, refer to the respective device documentation as listed in the related information section:

- For pin assignments information, refer to the device pin-out files.
- For the I/O standards features, refer to the device handbook I/O chapter.
- For the electrical specifications, refer to the device datasheet or DC and switching characteristics document.

Related Links

- [Stratix V Pin-Out Files](#)
- [Stratix IV Pin-Out Files](#)
- [Stratix III Device Pin-Out Files](#)
- [Intel Arria 10 Device Pin-Out Files](#)
- [Arria V Device Pin-Out Files](#)
- [Arria II GX Device Pin-Out Files](#)
- [Intel Cyclone 10 GX Device Pin-Out Files](#)
- [Intel Cyclone 10 LP Device Pin-Out Files](#)
- [Cyclone V Device Pin-Out Files](#)
- [Cyclone IV Device Pin-Out Files](#)
- [Cyclone III Device Pin-Out Files](#)
- [Intel MAX 10 Device Pin-Out Files](#)
- [I/O Features in Stratix V Devices](#)
- [I/O Features in Stratix IV Device](#)
- [Stratix III Device I/O Features](#)
- [I/O Features in Stratix V Devices](#)
- [I/O Features in Stratix IV Device](#)
- [Stratix III Device I/O Features](#)



- [I/O and High Speed I/O in Intel Arria 10 Devices](#)
- [I/O Features in Arria V Devices](#)
- [I/O Features in Arria II Devices](#)
- [I/O and High Speed I/O in Intel Cyclone 10 GX Devices](#)
- [I/O and High Speed I/O in Intel Cyclone 10 LP Devices](#)
- [I/O Features in Cyclone V Devices](#)
- [I/O Features in Cyclone IV Devices](#)
- [I/O Features in the Cyclone III Device Family](#)
- [Intel MAX 10 General Purpose I/O User Guide](#)
- [Stratix V Device Datasheet](#)
- [DC and Switching Characteristics for Stratix IV Devices](#)
- [Stratix III Device Datasheet: DC and Switching Characteristics](#)
- [Intel Arria 10 Device Datasheet](#)
- [Arria V Device Datasheet](#)
- [Device Datasheet for Arria II Devices](#)
- [Intel Cyclone 10 GX Device Datasheet](#)
- [Intel Cyclone 10 LP Device Datasheet](#)
- [Cyclone V Device Datasheet](#)
- [Cyclone IV Device Datasheet](#)
- [Cyclone III Device Datasheet](#)
- [Intel MAX 10 Device Datasheet](#)

BLVDS Power Consumption

In comparison to other high-performance bus technologies such as Gunning Transceiver Logic (GTL), which uses more than 40 mA, BLVDS typically drives out current in the range of 10 mA. For example, based on the Cyclone III Early Power Estimator (EPE) estimation for typical power characteristics of Cyclone III devices in an ambient temperature of 25° C, the average power consumption of a BLVDS bidirectional buffer at a data rate of 50 MHz and an output enabled 50% of the time is approximately 17 mW.

- Before implementing your design into the device, use the Excel-based EPE for the supported device you use to get an estimated magnitude of the BLVDS I/O power consumption.
- For input and bidirectional pins, the BLVDS input buffer is always enabled. The BLVDS input buffer consumes power if there is switching activity on the bus (for example, other transceivers are sending and receiving data, but the Cyclone III device is not the intended recipient).
- If you use BLVDS as an input buffer in multidrop or as a bidirectional buffer in multipoint applications, Intel recommends entering a toggle rate that includes all activities on the bus, not just activities intended for the Intel device BLVDS input buffer.



Figure 5. Example of BLVDS I/O Data Entry in the EPE

This figure shows the BLVDS I/O entry in the Cyclone III EPE. For I/O standards to select in the EPE of other supported Intel devices, refer to the related information.

I/O Standard	Current Strength / Output Termination	Slew Rate	# Input Pins	# Output Pins	# Bidir Pins	Data Rate	Clock Freq (MHz)	Toggle %	OE %	Load (pF)	Thermal Power (W)			Supply Current (A)	
											Routing	Block	Total	I _{CCINT}	I _{CCIO}
Bus LVDS	12mA	2	0	0	10	SDR	100.0	50.0%	50.0%	5	0.001	0.165	0.166	0.012	0.103
2.5 V	4mA	2	0	0	0	SDR	400.0	50.0%	100.0%	5	0.000	0.000	0.000	0.000	0.000

Intel recommends that you use the Intel Quartus Prime Power Analyzer Tool to perform an accurate BLVDS I/O power analysis after you complete your design. The Power Analyzer Tool estimates power based on the specifics of the design after place-and-route is completed. The Power Analyzer Tool applies a combination of user-entered, simulation-derived, and estimated signal activities which, combined with the detailed circuit models, yields very accurate power estimates.

Related Links

- [Power Analysis chapter, Intel Quartus Prime Pro Edition Handbook](#)
Provides more information about the Intel Quartus Prime Pro Edition Power Analyzer tool for the Intel Arria 10 and Intel Cyclone 10 GX device families.
- [Power Analysis chapter, Intel Quartus Prime Standard Edition Handbook](#)
Provides more information about the Intel Quartus Prime Standard Edition Power Analyzer tool for the Stratix V, Stratix IV, Stratix III, Arria V, Arria II, Intel Cyclone 10 LP, Cyclone V, Cyclone IV, Cyclone III LS, Cyclone III, and Intel MAX 10 device families.
- [Early Power Estimators \(EPE\) and Power Analyzer page](#)
Provides more information about the EPE and the Intel Quartus Prime Power Analyzer tool.
- [Implementing Bus LVDS Interface in Supported Intel FPGA Device Families on page 3](#)
Lists the I/O standards to select in the EPE to estimate the BLVDS power consumption.

BLVDS Design Example

The design example shows you how to instantiate the BLVDS I/O buffer in the supported devices with the relevant general purpose I/O (GPIO) IP cores in the Intel Quartus Prime software.

- Intel Arria 10 and Intel Cyclone 10 GX devices—use the Intel FPGA GPIO IP core.
- Intel MAX 10 devices—use the Intel FPGA GPIO Lite IP core.
- All other supported devices—use the ALTIIOBUF IP core.

You can download the design example from the link in the related information.



For the BLVDS I/O buffer instance, Intel recommends the following items:

- Implement the GPIO IP core in bidirectional mode with the differential mode turned on.
- Assign the I/O standard to the bidirectional pins:
 - BLVDS—Intel Cyclone 10 LP, Cyclone IV, Cyclone III, and Intel MAX 10 devices.
 - Differential SSTL-2 Class I or Class II—Stratix V, Stratix IV, Stratix III, Arria V, Arria II, and Cyclone V devices.
 - Differential SSTL-18 Class I or Class II—Intel Arria 10 and Intel Cyclone 10 GX devices.

Table 3. Input or Output Buffers Operation During Write and Read Operations

Write Operation (BLVDS I/O Buffer)	Read Operation (Differential Input Buffer)
<ul style="list-style-type: none"> • Receive a serial data stream from the FPGA core through the <code>doutp</code> input port • Create an inverted version of the data • Transmit the data through the two single-ended output buffers connected to the <code>p</code> and <code>n</code> bidirectional pins 	<ul style="list-style-type: none"> • Receive the data from the bus through the <code>p</code> and <code>n</code> bidirectional pins • Sends the serial data to the FPGA core through the <code>din</code> port

- The `oe` port receives the `oe` signal from the device core to enable or disable the single-ended output buffers.
- Keep the `oe` signal low to tri-state the output buffers during read operation.
- The function of the AND gate is to stop the transmitted signal from going back into the device core. The differential input buffer is always enabled.

Related Links

- [I/O Buffer \(ALTIobuf\) IP Core User Guide](#)
- [Intel FPGA GPIO IP Core User Guide](#)
- [Intel MAX 10 I/O Implementation Guides](#)
- [Introduction to Intel FPGA IP Cores](#)
- [Design Examples for AN 522](#)
Provides the Intel Quartus Prime design examples used in this application note.

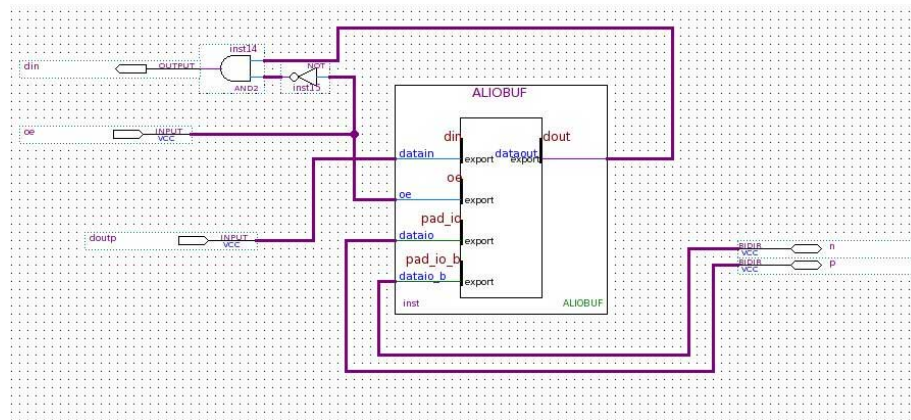
Design Example Guidelines for Intel Arria 10 and Intel Cyclone 10 GX Devices

These steps are applicable to Intel Arria 10 and Intel Cyclone 10 GX devices only. Ensure that you use the Intel FPGA GPIO IP core.

1. Open the `StratixV_blvds.qar` file to import the Stratix V design example into the Intel Quartus Prime Pro Edition software.
2. Migrate the design example to use the Intel FPGA GPIO IP core:
 - a. On the menu, select **Project > Upgrade IP Components**.
 - b. Double click the "ALIOBUF" entity. The **MegaWizard Plug-In Manager** window for the ALTIobuf IP core appears.
 - c. Turn off **Match project/default**.

- d. In **Currently selected device family**, select **Arria 10**.
 - e. Click **Finish** and then click **Finish** again.
 - f. In the dialog box that appears, click **OK**.
The Intel Quartus Prime Pro Edition software performs the migration process and then displays the Intel FPGA GPIO IP parameter editor.
3. Configure the Intel FPGA GPIO IP core to support a bidirectional input and output buffer:
 - a. In **Data Direction**, select **Bidir**.
 - b. In **Data width**, enter 1.
 - c. Turn on **Use differential buffer**.
 - d. Click **Finish** and generate the IP core.
 4. Connect the modules and the input and output ports as shown in the following figure:

Figure 6. Input and Output Ports Connection Example for Intel Arria 10 and Intel Cyclone 10 GX Devices



5. In the Assignment Editor, assign the relevant I/O standard as shown in the following figure. You can also set the current strength and slew rate options. Otherwise, the Intel Quartus Prime Pro Edition software assumes the default settings for Intel Arria 10 or Intel Cyclone 10 GX devices—Differential SSTL-18 Class I or Class II I/O standard.

Figure 7. BLVDS I/O Assignment in the Intel Quartus Prime Assignment Editor for Intel Arria 10 and Intel Cyclone 10 GX Devices

From	To	Assignment Name	Value	Enabled
	p	I/O Standard	Differential 1.8-V SSTL	Yes
	n	I/O Standard	Differential 1.8-V SSTL	Yes
	p	Current Strength	8MA	Yes
	n	Current Strength	8MA	Yes

Note: For Intel Arria 10 or Intel Cyclone 10 GX devices, you can manually assign both the p and n pin locations for LVDS pins with the Assignment Editor.

6. Compile and perform functional simulation with the ModelSim* - Intel FPGA Edition software.



Related Links

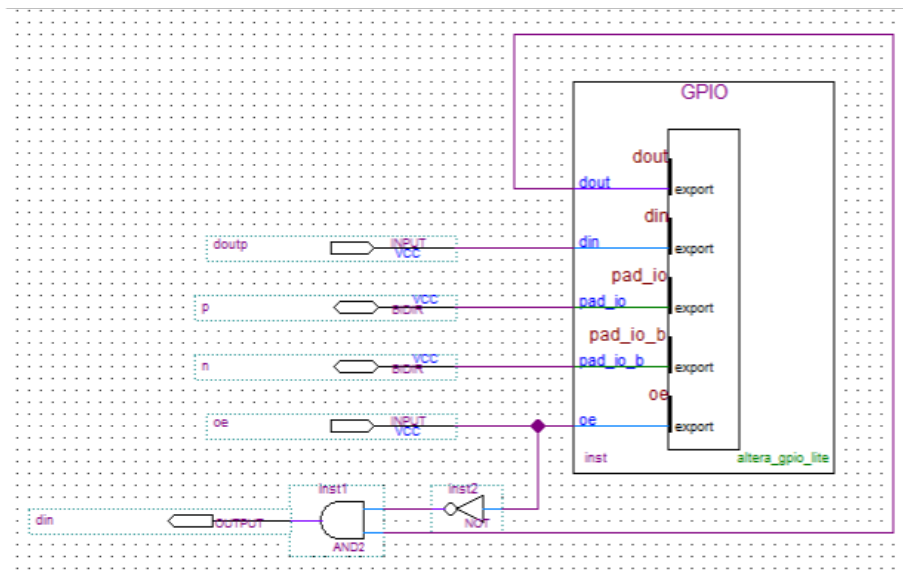
- [ModelSim - Intel FPGA Edition Software Support](#)
Provides more information about the ModelSim - Intel FPGA Edition software and contains various links to topics such as installation, usage, and troubleshooting.
- [I/O Standards for BLVDS Interface in Intel FPGA Devices](#) on page 7
Lists the pins and I/O standards you can manually assign in the supported Intel FPGA devices for BLVDS applications.

Design Example Guidelines for Intel MAX 10 Devices

These steps are applicable to Intel MAX 10 devices only. Ensure that you use the Intel FPGA GPIO Lite IP core.

1. Create an Intel FPGA GPIO Lite IP core that can support a bidirectional input and output buffer:
 - a. Instantiate the Intel FPGA GPIO Lite IP core.
 - b. In **Data Direction**, select **Bidir**.
 - c. In **Data width**, enter 1.
 - d. Turn on **Use pseudo differential buffer**.
 - e. In **Register mode**, select **Bypass**.
2. Connect the modules and the input and output ports as shown in the following figure:

Figure 8. Input and Output Ports Connection Example for Intel MAX 10 Devices



3. In the Assignment Editor, assign the relevant I/O standard as shown in the following figure. You can also set the current strength and slew rate options. Otherwise, the Intel Quartus Prime software assumes the default settings.

Figure 9. BLVDS I/O Assignment in the Intel Quartus Prime Assignment Editor for Intel MAX 10 Devices

From	To	Assignment Name	Value	Enabled
	io p	I/O Standard	Bus LVDS	Yes
	io p	Slew Rate	2	Yes
	io p	Current Strength	8mA	Yes
	io n	I/O Standard	Bus LVDS	Yes
	io n	Slew Rate	2	Yes
	io n	Current Strength	8mA	Yes

4. Compile and perform functional simulation with the ModelSim - Intel FPGA Edition software.

Related Links

- [ModelSim - Intel FPGA Edition Software Support](#)
Provides more information about the ModelSim - Intel FPGA Edition software and contains various links to topics such as installation, usage, and troubleshooting.
- [I/O Standards for BLVDS Interface in Intel FPGA Devices](#) on page 7
Lists the pins and I/O standards you can manually assign in the supported Intel FPGA devices for BLVDS applications.

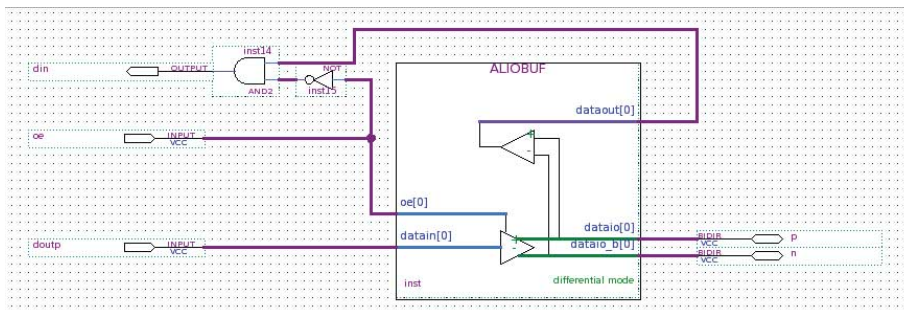
Design Example Guidelines for All Supported Devices Except Intel Arria 10, Intel Cyclone 10 GX, and Intel MAX 10

These steps are applicable to all supported devices except Intel Arria 10, Intel Cyclone 10 GX, and Intel MAX 10. Ensure that you use the ALTIOBUF IP core.

1. Create an ALTIOBUF IP core that can support a bidirectional input and output buffer:
 - a. Instantiate the ALTIOBUF IP core.
 - b. Configure the module **As a bidirectional buffer**.
 - c. In **What is the number of buffers to be instantiated**, enter 1.
 - d. Turn on **Use differential mode**.
2. Connect the modules and the input and output ports as shown in the following figure:



Figure 10. Input and Output Ports Connection Example for All Supported Devices Except Intel Arria 10, Intel Cyclone 10 GX, and Intel MAX 10 Devices



3. In the Assignment Editor, assign the relevant I/O standard as shown in the following figure according to your device. You can also set the current strength and slew rate options. Otherwise, the Intel Quartus Prime software assumes the default settings.
 - Intel Cyclone 10 LP, Cyclone IV, Cyclone III, and Cyclone III LS devices—BLVDS I/O standard to the bidirectional p and n pins as shown in the following figure.
 - Stratix V, Stratix IV, Stratix III, Arria V, Arria II, and Cyclone V devices—Differential SSTL-2 Class I or Class II I/O standard.

Figure 11. BLVDS I/O Assignment in the Intel Quartus Prime Assignment Editor

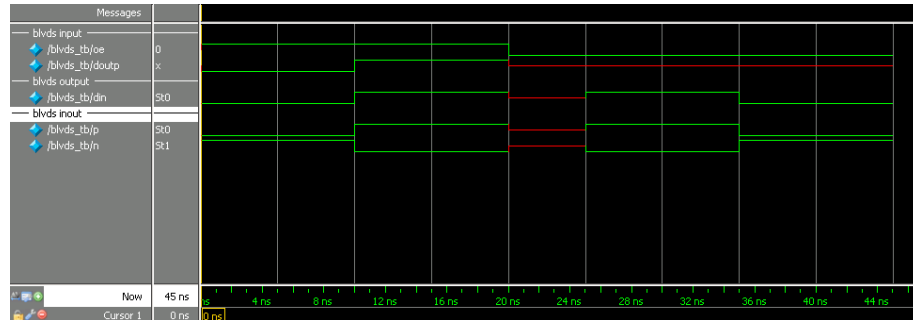
From	To	Assignment Name	Value	Enabled
	p	I/O Standard	Bus LVDS	Yes
	n	I/O Standard	Bus LVDS	Yes
	p	Slew Rate	2	Yes
	n	Slew Rate	2	Yes
	p	Current Strength	8MA	Yes
	n	Current Strength	8MA	Yes
	p	Location	PIN_T19	Yes
	n	Location	PIN_T20	Yes

Note: You can manually assign both the p and n pin locations for each supported device with the Assignment Editor. For the supported devices and the pins you can manually assign, refer to the related information.

4. Compile and perform functional simulation with the ModelSim - Intel FPGA Edition software.

Figure 12. Example of Functional Simulation Results

When the `oe` signal is asserted, the BLVDS is in write operation mode. When the `oe` signal is deasserted, the BLVDS is in read operation mode.



Note: For simulation using Verilog HDL, you can use the `blvds_tb.v` testbench, which is included in the respective design example.

Related Links

- [ModelSim - Intel FPGA Edition Software Support](#)
Provides more information about the ModelSim - Intel FPGA Edition software and contains various links to topics such as installation, usage, and troubleshooting.
- [I/O Standards for BLVDS Interface in Intel FPGA Devices](#) on page 7
Lists the pins and I/O standards you can manually assign in the supported Intel FPGA devices for BLVDS applications.

Performance Analysis

The multipoint BLVDS performance analysis demonstrates the impact of the bus termination, loading, driver and receiver characteristics, and the location of the receiver from the driver on the system.

You can use the included BLVDS design examples to analyze the performance of a multipoint application:

- Cyclone III BLVDS design example—this design example is applicable to all supported Stratix, Arria, and Cyclone device series. For Intel Arria 10 or Intel Cyclone 10 GX device family, you need to migrate the design example to the respective device family first before you can use it.
- Intel MAX 10 BLVDS design example—this design example is applicable to Intel MAX 10 device family.

Note: The performance analysis of a multipoint BLVDS in this section is based on the Cyclone III BLVDS input/output buffer information specification (IBIS) model simulation in HyperLynx*.



Intel recommends that you use these Intel IBIS models for simulation:

- Stratix III, Stratix IV, and Stratix V devices—device-specific Differential SSTL-2 IBIS model
- Intel Arria 10⁽²⁾ and Intel Cyclone 10 GX devices:
 - Output buffer—Differential SSTL-18 IBIS model
 - Input buffer—LVDS IBIS model

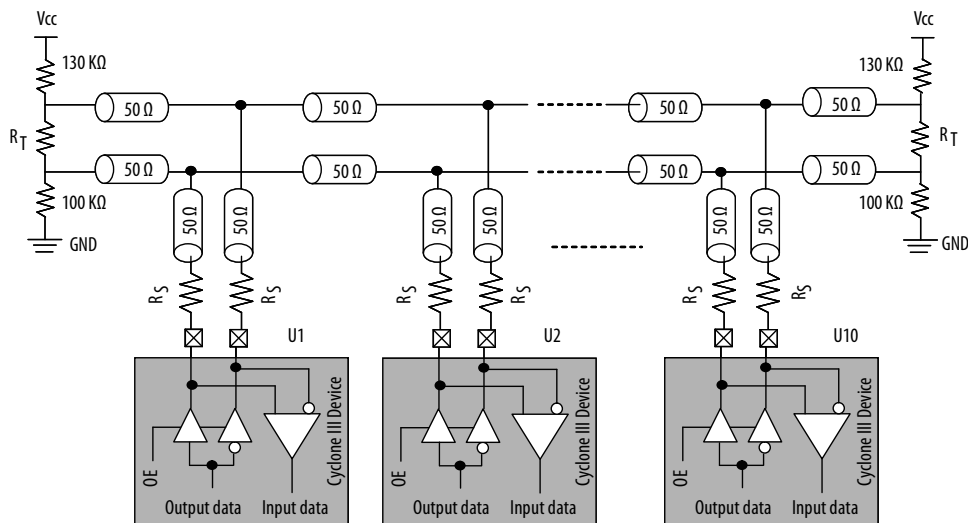
Related Links

- [Intel FPGA IBIS Model page](#)
Provides downloads of Intel FPGA device models.
- [Design Examples for AN 522](#)
Provides the Intel Quartus Prime design examples used in this application note.

System Setup

Figure 13. Multipoint BLVDS with Cyclone III BLVDS Transceivers

This figure shows the schematic of a multipoint topology with ten Cyclone III BLVDS transceivers (named U1 to U10).



The bus transmission line is assumed to have the following characteristics:

- A stripline
- Characteristic impedance of 50 Ω
- Characteristic capacitance of 3.6 pF per inch
- Length of 10 inches
- Bus differential characteristic impedance of approximately 100 Ω
- Spacing between each transceiver of 1 inch
- Bus terminated at both ends with termination resistor R_T

⁽²⁾ The Intel Arria 10 IBIS models are preliminary and are not available on the Intel IBIS model web page. If you require these preliminary Intel Arria 10 IBIS models, contact Intel.



In the example shown in the preceding figure, the fail-safe biasing resistors of 130 k Ω and 100 k Ω pulls the bus to a known state when all the drivers are tri-stated, removed, or powered off.

To prevent excessive loading to the driver and waveform distortion, the magnitude of the fail-safe resistors must be one or two orders higher than R_T . To prevent a large common-mode shift from occurring between the active and tri-state bus conditions, the mid-point of the fail-safe bias must be close to the offset voltage of the driver (+1.25 V). You can power up the bus with the common power supplies (V_{CC}).

Cyclone III, Cyclone IV, and Intel Cyclone 10 LP BLVDS transceivers are assumed to have the following characteristics:

- Default drive strength of 12 mA
- Slow slew rate settings by default
- Pin capacitance of each transceiver of 6 pF
- Stub on each BLVDS transceiver is a 1-inch microstrip of characteristic impedance of 50 Ω and characteristic capacitance of 3 pF per inch
- Capacitance of the connection (connector, pad, and via in PCB) of each transceiver to the bus is assumed to be 2 pF
- Total capacitance of each load is approximately 11 pF

For 1-inch load spacing, the distributed capacitance is equal to 11 pF per inch. To reduce reflection caused by the stubs, and also to attenuate the signals coming out of the driver, an impedance matching 50 Ω resistor R_S is placed at the output of each transceiver.

Bus Termination

The effective impedance of the fully loaded bus is 52 Ω if you substitute the bus characteristic capacitance and the distributed capacitance per unit length of the setup into the effective differential impedance equation. For optimum signal integrity, you must match R_T to 52 Ω .

The following figures show the effects of matched-, under-, and over-termination on the differential waveform (V_{ID}) at the receiver input pins. The data rate is 100 Mbps. In these figures, under-termination ($R_T = 25 \Omega$) results in reflections and significantly reduction of the noise margin. In some cases, under termination even violates the receiver threshold ($V_{TH} = \pm 100$ mV). When R_T is changed to 50 Ω , there is a substantial noise margin with respect to V_{TH} and the reflection is negligible.



Figure 14. Effect of Bus Termination (Driver in U1, Receiver in U2)

In this figure, U1 acts as the transmitter and U2 to U10 are the receivers.

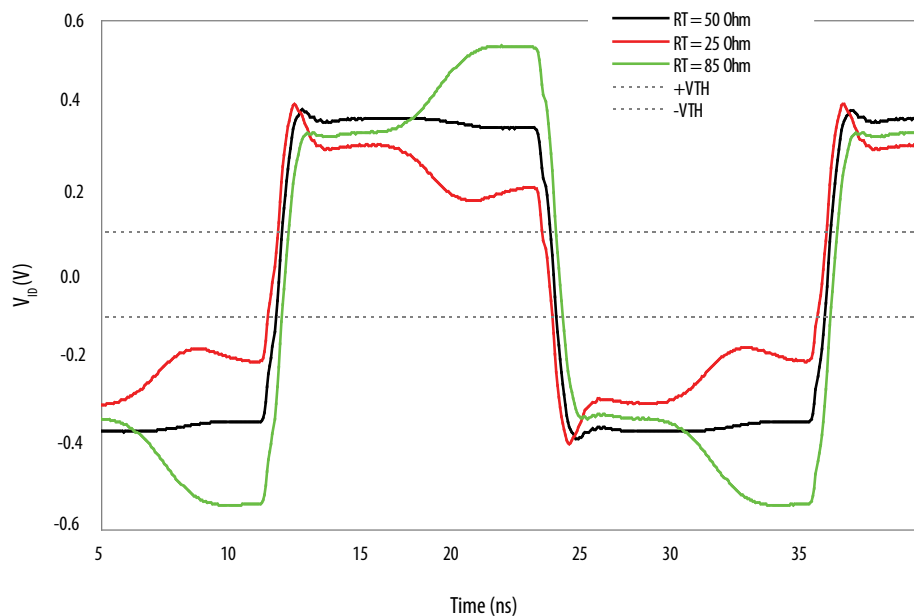


Figure 15. Effect of Bus Termination (Driver in U1, Receiver in U10)

In this figure, U1 acts as the transmitter and U2 to U10 are the receivers.

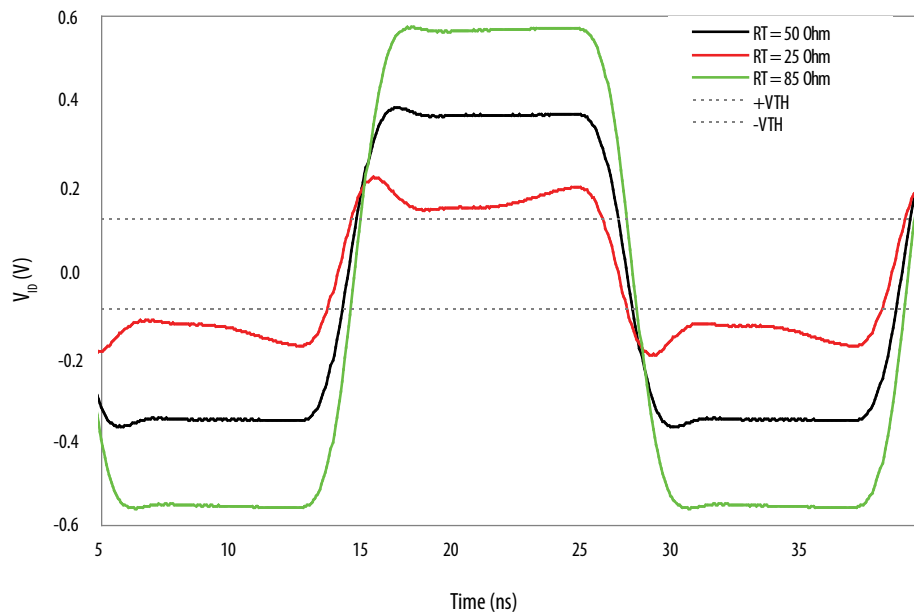


Figure 16. Effect of Bus Termination (Driver in U5, Receiver in U6)

In this figure, U5 is the transmitter and the rest are receivers.

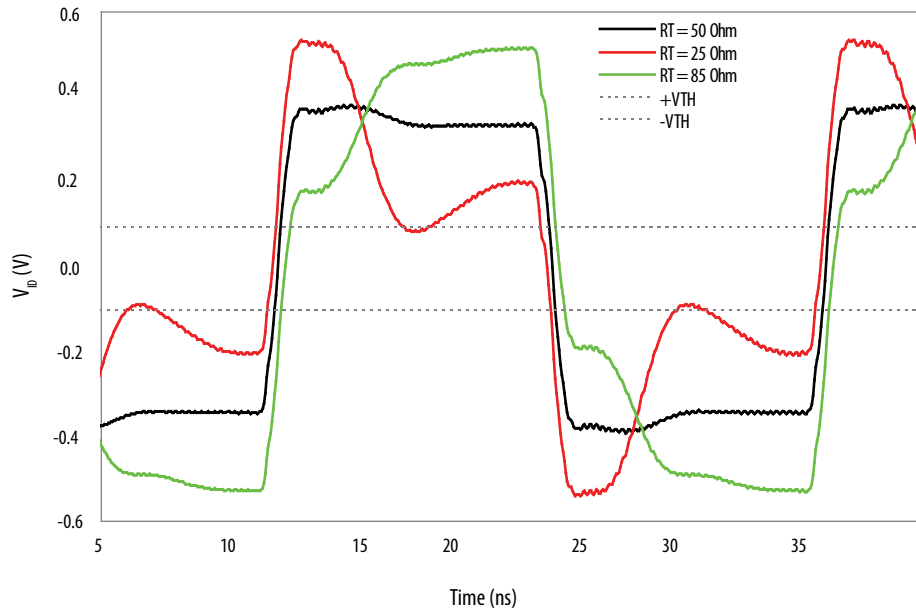
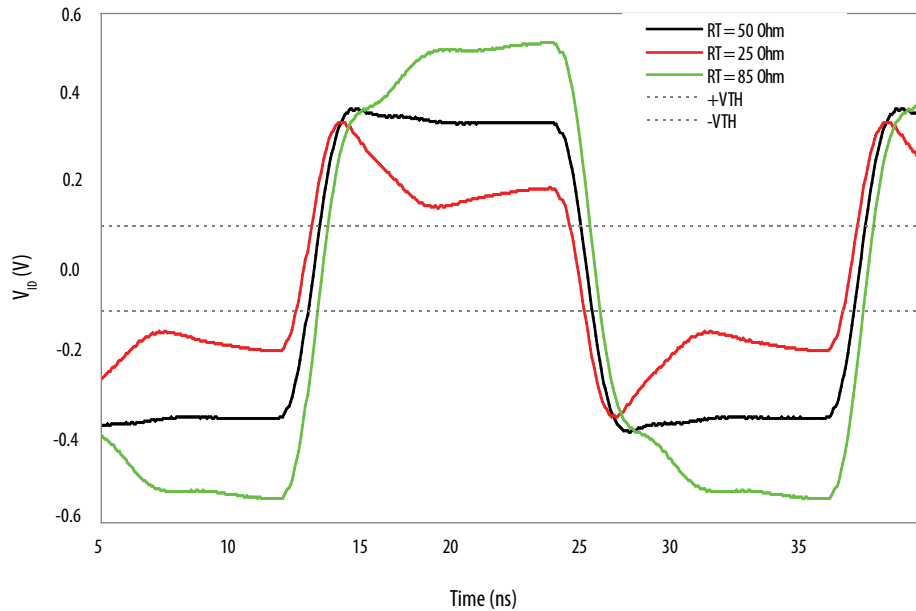


Figure 17. Effect of Bus Termination (Driver in U5, Receiver in U10)

In this figure, U5 is the transmitter and the rest are receivers.



The relative position of the driver and receiver on the bus also affects the received signal quality. The nearest receiver to the driver experiences the worst transmission line effect because at this location, the edge rate is the fastest. This is made worse when the driver is located at the middle of the bus.



For example, compare [Figure 15](#) on page 19 and [Figure 17](#) on page 20. V_{ID} at receiver U6 (driver at U5) shows larger ringing than that at receiver U2 (driver at U1). On the other hand, the edge rate is slowed down when the receiver is located further away from the driver. The largest rise time recorded is 1.14 ns with the driver located at one end of the bus (U1) and the receiver at the other end (U10).

Related Links

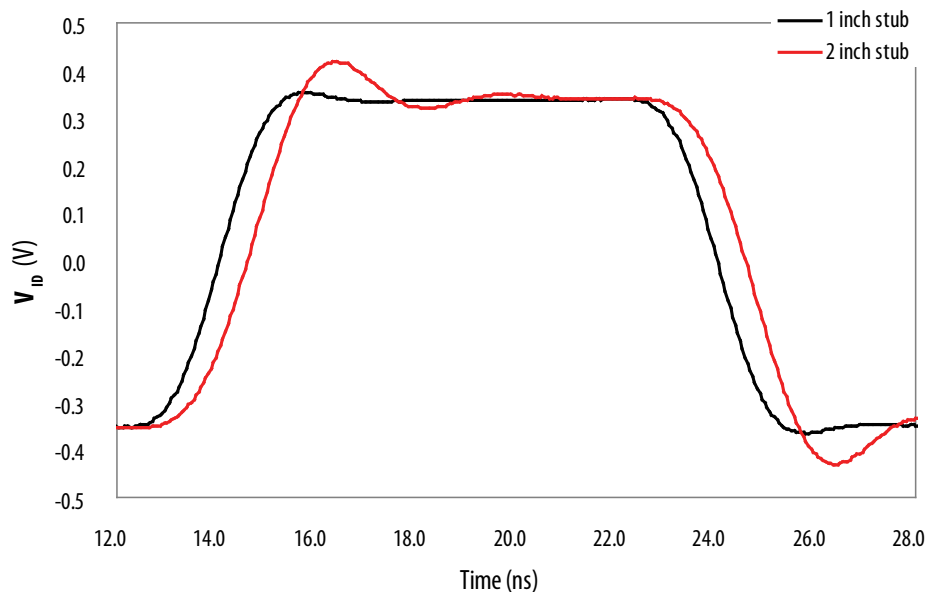
[Effective Impedance](#) on page 4

Stub Length

Longer stub length not only increases the flight time from the driver to the receiver, but also results in a larger load capacitance, which causes larger reflection.

Figure 18. Effect of Increasing Stub Length (Driver in U1, Receiver in U10)

This figure compares the V_{ID} at U10 when the stub length is increased from one inch to two inches and the driver is at U1.

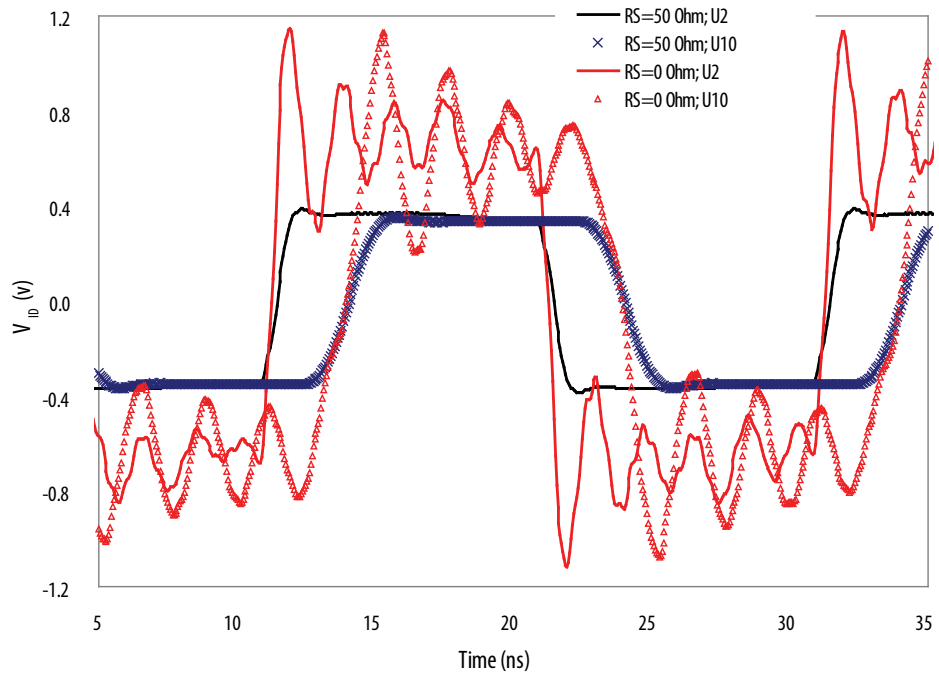


Stub Termination

You must match the driver impedance to the stub characteristic impedance. Placing a series termination resistor R_S at the driver output greatly reduces the adverse transmission line effect caused by long stub and fast edge rates. In addition, R_S can be changed to attenuate the V_{ID} to meet the specification of the receiver.

Figure 19. Effect of Stub Termination (Driver in U1, Receiver in U2 and U10)

This figure compares the V_{ID} at U2 and U10 when U1 is transmitting.



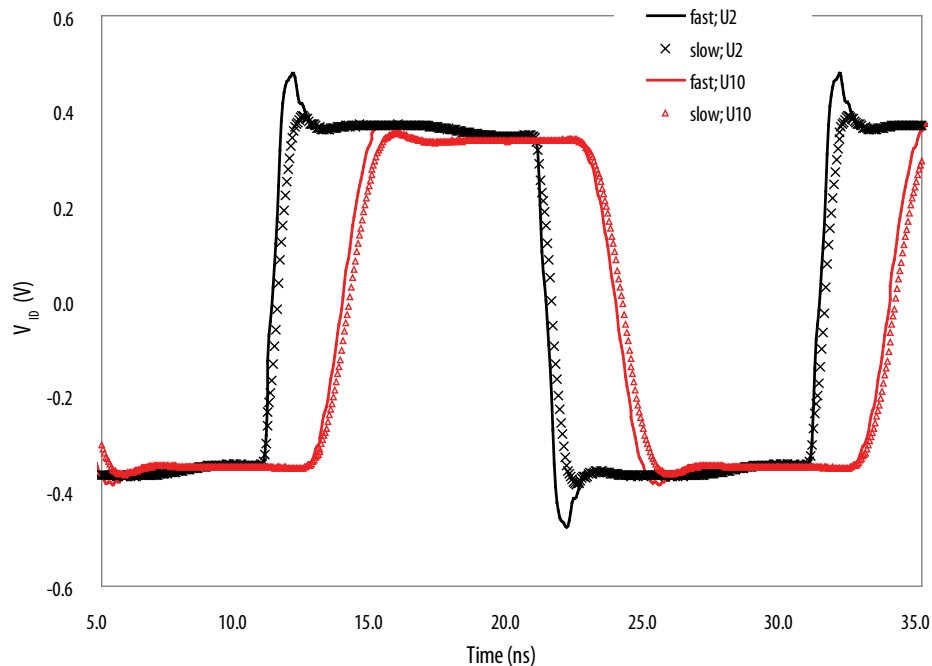
Driver Slew Rate

A fast slew rate helps to improve the rise time, especially at the receiver furthest from the driver. However, a faster slew rate also magnifies ringing due to reflection.



Figure 20. Effect of Driver Edge Rate (Driver in U1, Receiver in U2 and U10)

This figure shows the driver slew rate effect. A comparison is made between the slow and fast slew rate with a 12 mA drive strength. The driver is at U1 and the differential waveforms at U2 and U10 are examined.



Overall System Performance

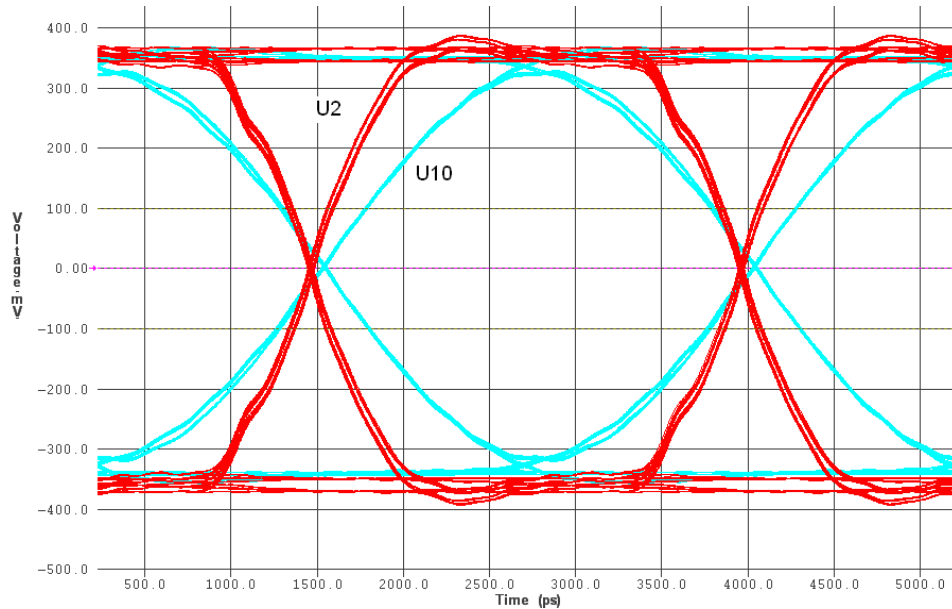
The highest data rate supported by a multipoint BLVDS is determined by looking at the eye diagram of the furthest receiver from a driver. At this location, the transmitted signal has the slowest edge rate and affects the eye opening.

Although the quality of the received signal and the noise margin goal depend on the applications, the wider the eye opening, the better. However, you must also check the receiver nearest to the driver, because the transmission line effects tend to be worse if the receiver is located closer to the driver.



Figure 21. Eye Diagram at 400 Mbps (Driver in U1, Receiver in U2 and U10)

This figure illustrates the eye diagrams at U2 (red curve) and U10 (blue curve) for a data rate at 400 Mbps. Random jitter of a 1% unit interval is assumed in the simulation. The driver is at U1 with default current strength and slew rate settings. The bus is fully loaded with optimum $R_T = 50 \Omega$. The smallest eye opening is at U10, which is furthest from U1. The eye height sampled at the 0.5 unit interval is 692 mV and 543 mV for U2 and U10, respectively. There is a substantial noise margin with respect to $V_{TH} = \pm 100$ mV for both cases.



Document Revision History for AN 522: Implementing Bus LVDS Interface in Supported Intel FPGA Device Families

Date	Version	Changes
November 2017	2017.11.06	<ul style="list-style-type: none"> Added support for Intel Cyclone 10 LP devices. Updated related information links. Updated I/O standard names to follow standard usage. Rebranded as Intel, including names of devices, IP cores, and software tools, where applicable.
May 2016	2016.05.02	<ul style="list-style-type: none"> Added support and design example for Intel MAX 10 devices. Restructured several sections to improve clarity. Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.
June 2015	2015.06.09	<ul style="list-style-type: none"> Updated the design example files. Updated design example guidelines: <ul style="list-style-type: none"> Moved the steps for Arria 10 devices into a new topic. Added steps to migrate the design examples to use Altera GPIO IP core for Arria 10 devices. Updated the design example steps to match the updated design examples. Updated all links to updated website location and web-based documentation (if available).
August 2014	2014.08.18	<ul style="list-style-type: none"> Updated application note to add Arria 10 device support. Restructured and rewrote several sections for clarity and style update. Updated template.

continued...



Date	Version	Changes
June 2012	2.2	<ul style="list-style-type: none"> • Updated to include Arria II, Arria V, Cyclone V, and Stratix V devices. • Updated Table 1 and Table 2.
April 2010	2.1	Updated the design example link in the "Design Example" section.
November 2009	2.0	<ul style="list-style-type: none"> • Included Arria II GX, Cyclone III, and Cyclone IV device families in this application note. • Updated Table 1, Table 2, and Table 3. • Update Figure 5, Figure 6, Figure 8 through Figure 11. • Updated design example files.
November 2008	1.1	<ul style="list-style-type: none"> • Updated to new template • Updated "BLVDS Technology in Altera Devices" chapter • Updated "Power Consumption of BLVDS" chapter • Updated "Design Example" chapter • Replaced Figure 4 on page 7 • Updated "Design Example Guidelines" chapter • Updated "Performance Analysis" chapter • Updated "Bus Termination" chapter • Updated "Summary" chapter
July 2008	1.0	Initial release.