The Arria V® and Cyclone V Hard Processor System (HPS) provide two USB On-the-Go (OTG) controllers. Each USB 2.0 OTG controller supports a single USB port connected through a USB 2.0 Transceiver Macrocell Interface Plus (UTMI+) Low Pin Interface (ULPI) compliant PHY.

When interfacing your design to a USB PHY, it is important to do timing analysis to ensure that the interface between the USB controller and USB PHY works reliably across a range of process, voltage and temperature (PVT) variations.

Related Information

- **USB 2.0 OTG Controller**
  Chapter in the *Arria V Device Handbook, Volume 3*
- **USB 2.0 OTG Controller**
  Chapter in the *Cyclone V Device Handbook, Volume 3*
- **The Quartus II TimeQuest Timing Analyzer**

### ULPI Signals

#### Table 1: Signals Included in the ULPI Interface

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK</td>
<td>Interface clock—All signals are synchronous to the clock.</td>
</tr>
<tr>
<td>DATA[7:0]</td>
<td>Data bus—Driven low by the controller during idle. The controller starts a transfer by sending a non-zero pattern. The PHY must assert DIR before using the data bus. Every time DIR toggles, DATA must be ignored for one clock cycle (the turnaround cycle).</td>
</tr>
<tr>
<td>DIR</td>
<td>Direction of the data bus—By default, DIR is low and the PHY listens for non-zero data from the controller. The PHY asserts DIR to get control of the data bus.</td>
</tr>
<tr>
<td>NXT</td>
<td>Next data—The PHY drives NXT high to throttle the data bus.</td>
</tr>
<tr>
<td>STP</td>
<td>Stop data—The controller drives STP high to signal the end of the data stream. The controller can also drive STP high to request data bus access from the PHY.</td>
</tr>
</tbody>
</table>
HPS USB Timing Characteristics

The Arria V and Cyclone V Hard Processor System USB controllers have been characterized across a range of PVT variations. The following USB timing information appears in the Arria V and Cyclone V datasheets.

Related Information
- Cyclone V Device Datasheet
- Arria V Device Datasheet

USB Timing Requirements

**Table 2: HPS USB MAC Timing Requirements**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tclk</td>
<td>USB CLK clock period</td>
<td>-</td>
<td>16.67</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>MAC Td</td>
<td>CLK to USB_STP/USB_DATA[7:0] output delay</td>
<td>4.4</td>
<td>-</td>
<td>11.0</td>
<td>ns</td>
</tr>
<tr>
<td>MAC Tsu</td>
<td>Setup time for USB_DIR/USB_NXT/USB_DATA[7:0]</td>
<td>2.0</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>MAC Th</td>
<td>Hold time for USB_DIR/USB_NXT/USB_DATA[7:0]</td>
<td>1.0</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
</tbody>
</table>

USB Timing Diagram

![USB Timing Diagram](image)

PHY Selection

The timing characteristic of ULPI PHYs vary across the spectrum of available devices.

Arria V and Cyclone USB 2.0 OTG controllers support the following clock modes:
- Output clock mode—the PHY drives the clock to the controller
- Input clock mode—the PHY is driven by an external clock source on the board or a clock input sourced from the FPGA fabric.

Output clock mode is supported by all ULPI PHYs.
Input clock mode is supported by newer ULPI PHYs. This mode can be used to compensate for timing mismatches between the PHY and the controller.

### USB PHY Timing Characteristics

Before selecting a USB PHY and clock mode of operation, you should perform a timing analysis of the USB controller and PHY.

If the USB PHY supports both modes of operation with different timing characteristics, then a timing analysis of both modes should be performed before making a PHY selection. As an example, consider a system with the USB PHY in output clock mode and the following PHY and board delays:

#### Table 3: USB PHY Timing Requirements

The PHY timings listed below are from the MicroChip USB3300 PHY, which populates both the Arria V and Cyclone V SoC Development Boards. On the development board, this USB PHY operates in output clock mode.

**Note:** PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board.

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>PHY Tsu</td>
<td>PHY setup time for USB_STP/USB_DATA[7:0]</td>
<td>5.0</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>PHY Th</td>
<td>PHY hold time for USB_STP/USB_DATA[7:0]</td>
<td>0</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>PHY Td</td>
<td>Output delay for USB_DIR/USB_NXT/USB_DATA[7:0]</td>
<td>2.0</td>
<td>-</td>
<td>5.0</td>
<td>ns</td>
</tr>
<tr>
<td>ClkTrace Td</td>
<td>Clock Trace delay</td>
<td>0.05</td>
<td>-</td>
<td>0.1</td>
<td>ns</td>
</tr>
<tr>
<td>DTrace Td</td>
<td>Data Trace delay</td>
<td>0.05</td>
<td>-</td>
<td>0.1</td>
<td>ns</td>
</tr>
<tr>
<td>Clock Tu</td>
<td>Clock Source Uncertainty</td>
<td>-</td>
<td>0.3</td>
<td>-</td>
<td>ns</td>
</tr>
</tbody>
</table>

If the trace lengths of the DATA[7:0], STP and NXT signals are matched, then the following calculations verify that the USB timing is met off-chip:
• USB Controller to PHY setup time:

The sum of the maximum output delay of the USB MAC (as displayed in the USB MAC Timing Requirements table), the maximum data trace delay and the clock source uncertainty is subtracted from the USB clock period to determine if it is greater than or equal to the sum of the PHY setup time and the maximum clock trace delay. Because the clock source originates from the USB PHY in output clock mode, the clock trace delay must be added to the USB PHY setup time in this equation.

\[ T_{clk} - (MAC\ Td_{\text{max}} + DTrace\ Td_{\text{max}} + Clock\ Tu) \geq USB\ PHY\ Tsu + ClkTrace\ Td_{\text{max}} \]

\[ 16.67 - (11.0 + 0.1 + 0.3) \geq 5.0 + 0.1 \]

\[ 16.67 - 11.4 \geq 5.1 \]

\[ 5.27 \text{ ns} \geq 5.1 \text{ ns} \]

• USB Controller to PHY Hold

The USB MAC minimum output delay is added to the minimum trace delay to determine if it is greater than or equal to the USB PHY hold time requirement minus the minimum clock trace delay. Because the clock source originates from the USB PHY in output clock mode and adds delay to data arriving at the USB PHY, the minimum clock trace delay must be subtracted from the USB PHY hold time.

\[ USB\ MAC\ Td_{\text{min}} + Trace\ Td_{\text{min}} \geq USB\ PHY\ Th - ClkTrace\ Td_{\text{min}} \]

\[ 4.4 + 0.05 \geq 0 - 0.05 \]

\[ 4.45 \text{ ns} \geq -0.05 \text{ ns} \]

• USB PHY to USB Controller Setup:

The sum of the maximum output delay of the USB PHY (as displayed in the USB PHY Timing Requirements table), the trace delay difference and the clock source uncertainty is subtracted from the USB clock period to determine if it is greater than or equal to the USB MAC setup time. As the difference of the data trace delay to clock trace delay increases, the time that data is available to the USB MAC Controller is later.

\[ T_{clk} - (USB\ PHY\ Td_{\text{max}} + (DTrace\ Td_{\text{max}} - ClkTrace\ Td_{\text{max}}) + Clock\ Tu) \geq USB\ MAC\ Tsu \]

\[ 16.67 - (5.0 + (0.1 - 0.1) + 0.3) \geq 2.0 \]

\[ 11.37 \text{ ns} \geq 2.0 \text{ ns} \]

• USB PHY to USB Controller Hold:

The USB PHY minimum output delay is added to the difference of the minimum data trace delay and maximum clock trace delay to determine if it is greater than or equal to the USB MAC hold time requirement.

\[ USB\ PHY\ Td_{\text{min}} + (DTrace\ Td_{\text{min}} - ClkTrace\ Td_{\text{max}}) \geq USB\ MAC\ Th \]

\[ 2.0 + (0.05 - 0.1) \geq 1.0 \]

\[ 2.0 - 0.05 \geq 1.0 \]

\[ 1.95 \text{ ns} \geq 1.0 \text{ ns} \]

Output Clock Mode

In output clock mode, the clock is generated by the USB PHY. All signals are synchronized to this clock. To use this mode of operation, you must configure the USB Controller PHY interface mode for "SDR with PHY clock output mode" in the Peripheral Pins tab of HPS Parameters window in Qsys. This mode of operation configures the USB Controller clock pin to operate in an input mode.
Related Information

**Configuring the HPS USB 2.0 OTG Controller** on page 7
Refer to this section for more information on how to configure the USB interface in QSys.

### Input Clock Mode

In input clock mode, the PHY receives a clock from an external source. All signals are synchronized to the clock. In this mode, the clock can be generated by a PLL in the FPGA, or by an external source.

**Note:** For systems where the HPS must be operational before the FPGA fabric is configured, an external clock source should be used to drive the USB PHY clock. By using an external clock source, the FPGA fabric is not required to be configured before the HPS.

### External Clock Source

Although the USB PHY is configured in input clock mode, the clock source is still driven into the USB controller as an input to the SoC device. As a result, the USB controller must be configured for "SDR with PHY clock output mode" in the **Peripheral Pins** tab of the **HPS Parameters** window of Qsys. This mode of operation configures the USB Controller clock pin to operate as an input.
### Related Information

**Configuring the HPS USB 2.0 OTG Controller** on page 7

Refer to this section for more information on how to configure the USB interface in QSys.

### FPGA Clock Source

When the FPGA fabric drives the USB Controller clock output the USB interface requires the use of a loan I/O pin instead of the typical USB clock input pin.

User logic in the FPGA drives a clock signal, typically derived from a PLL, into the loan I/O assigned to the USB controller which is then routed into the USB controller and externally to the USB PHY. This configuration provides a common clock source for both the USB controller and PHY much like when the PHY is configured for input clock mode with an external clock source. Because this mode of operation differs from the previous scenarios, the USB controller must be configured for “SDR with PHY clock input mode” in the **Peripheral Pins** tab of the **HPS Parameters** window of Qsys.
Caution: When implementing input clock mode with an FPGA clock source, the FPGA must be configured prior to USB interface operation. This implementation option can have significant impacts to embedded software and must be considered carefully before selecting the input clock mode with FPGA clock source. Using an external clock source (as shown in Figure 2) can accomplish the same objective without necessarily affecting embedded software.

Related Information

**Configuring the HPS USB 2.0 OTG Controller** on page 7
Refer to this section for more information on how to configure the USB interface in QSys.

**Implementing Input Clock Mode with FPGA Clock Source**

The following example details how to configure the FPGA to the HPS USB Controller and the external USB PHY by using a Loan I/O in the HPS.

**Configuring the HPS USB 2.0 OTG Controller**

1. In the **Peripheral Pins** tab of the Hard Processor System parameter editor, select a USB controller by setting either **USB0 pin** or **USB1 pin** to one of the available HPS I/O pin sets.
2. Select the PHY interface mode in the corresponding list, **USB0 PHY interface mode** or **USB1 PHY interface mode**. Set the mode to **SDR with PHY clock input mode**.
Select the Controller Clock as Loan I/O

On the **Peripheral Pins** tab, scroll down to the **Peripherals Mux Table** to select the USB clock pin as loan I/O. This setting allows a clock from a PLL in the FPGA to connect to the USB controller.

Refer to the following table for the appropriate loan I/O for each USB option.

**Table 4: USB Loan I/O**

<table>
<thead>
<tr>
<th>USB I/O Pin Set</th>
<th>Loan I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB0 I/O Set 0</td>
<td>LOANIO44</td>
</tr>
<tr>
<td>USB1 I/O Set 0</td>
<td>LOANIO10</td>
</tr>
<tr>
<td>USB1 I/O Set 1</td>
<td>LOANIO29</td>
</tr>
</tbody>
</table>

**Connecting the Clock in the Top Level Design**

The following example shows how to connect the FPGA clock to a Loan I/O when the USB PHY is configured in input clock mode using an FPGA clock source from the SoC.

Add the following code snippets to your top-level design file, to connect the clock outputs to the loan I/O:

```vhdl
// top level module pin defines
// LOANIO10 = mac clock
inout wire LOANIO10,
```
// wire instances of the 3 loan IO buses from Qsys instance
wire [66:0] loan_out;
wire [66:0] loan_oe;

// this synthesis keep directive is required in
// order to connect PLL clock outputs to the Loan IO
wire        usb_mac_clk_from_pll    /* synthesis keep */;

// make assignment of the clocks to the appropriate loan IO
assign loan_out[10]   = usb_mac_clk_from_pll;
assign loan_oe[10]    = 1'b1;

// snippet of Qsys instantiation signal assignments
.hps_0_h2f_loan_io_in                  (),         // hps_0_h2f_loan_io.in
.hps_0_h2f_loan_io_out                 (loan_out),    //                  .out
.hps_0_h2f_loan_io_oe                  (loan_oe),     //                  .oe
.hps_io_0_hps_io_gpio_inst_LOANIO10    (LOANIO10),    // hps_io_gpio_inst_LOANIO10

Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>July 2014</td>
<td>2014.07.21</td>
<td>• Corrected the USB MAC Th number value in the USB PHY to USB Controller Hold equation in the USB PHY Timing Characteristics section.</td>
</tr>
<tr>
<td>July 2014</td>
<td>2014.07.16</td>
<td>• Corrected the ClkTrace Td_max value in the USB PHY to USB Controller Setup equation in the USB PHY Timing Characteristics section.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Corrected the USB PHY Td_min value in the USB PHY to USB Controller Hold equation in the USB PHY Timing Characteristics section.</td>
</tr>
<tr>
<td>July 2014</td>
<td>2014.07.03</td>
<td>• Modified Table 2: USB MAC Timing Requirements.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added USB PHY Timing Characteristics section.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Clarified Output Clock Mode section.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Modified Input Clock Mode section.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Removed Two Clock Mode, Selecting the PHY Clock, Instantiating a PLL, and Constraining the Design sections.</td>
</tr>
</tbody>
</table>