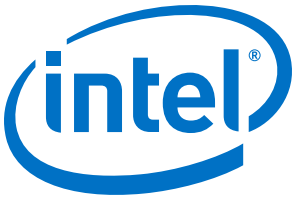


# AN 746: SDI II Triple-Rate Reference Designs for Intel® Arria® 10 Devices

*AN-746*
*2017.05.08*

# Contents

# 1 Triple Rate SDI II Reference Designs for Intel® Arria® 10 Devices

The triple rate Serial Digital Interface II (SDI II) reference designs demonstrate the transmission and reception of video data using the SDI II IP core and theArria® 10 GX FPGA Development Kit.

Intel offers the following reference designs:

- Triple Rate SDI II with External voltage-controlled crystal oscillator (VCXO) Reference Design for Arria 10 Devices
  - Uses one duplex and one simplex TX of the triple-rate SDI II IP core.
  - Supports SD-SDI, HD-SDI, and 3G-SDI standards.
- Triple Rate SDI II VCXO Removal Reference Design for Arria 10 Devices
  - Uses one simplex TX and one simplex RX of the triple-rate SDI II IP core.
  - Supports SD-SDI, HD-SDI, and 3G-SDI standards.

This application note describes the design components and requirements. It also includes the instructions on setting up and testing the reference designs.

### Related Links

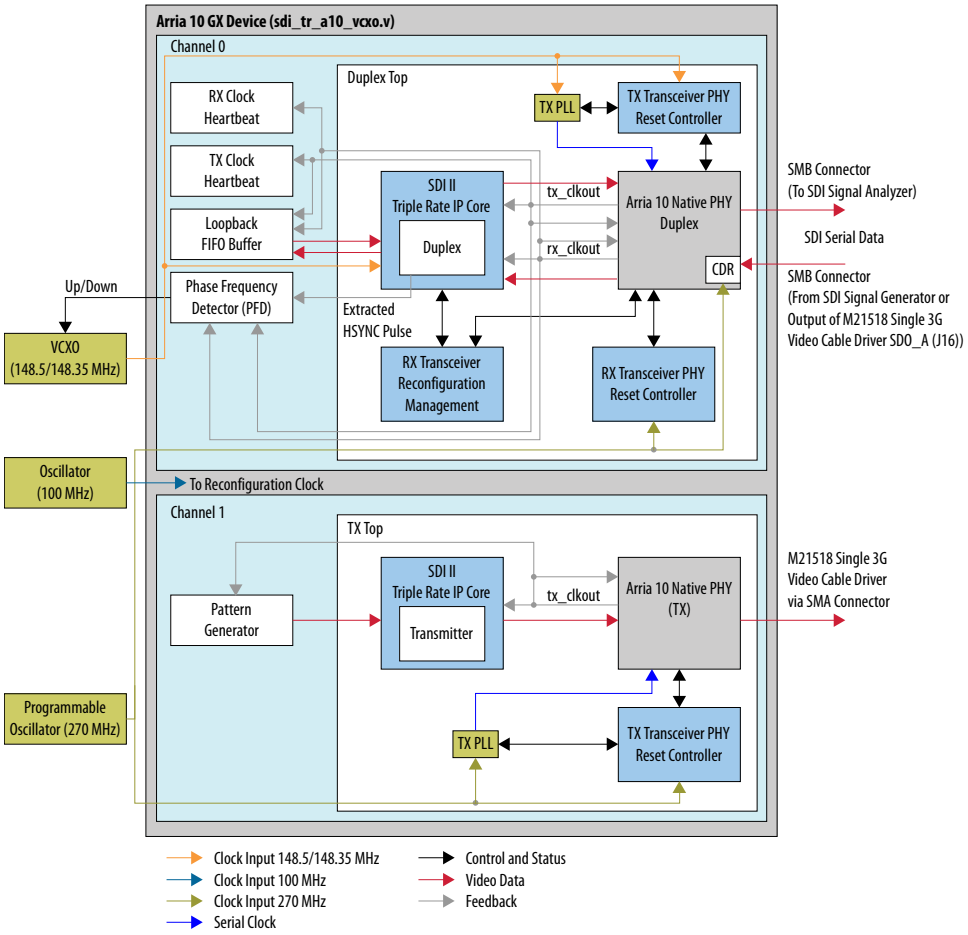
- Triple Rate SDI II with External VCXO Reference Design 16.0
  Provides the design files for this reference design.
- Triple Rate SDI II with VCXO Removal Reference Design 16.0
  Provides the design files for this reference design.

## 1.1 Triple Rate SDI II with External VCXO Reference Design

This reference design consists of two channels: channel 0—SDI II IP in duplex mode and channel 1—SDI II IP core configured as a transmitter. In Arria 10 devices, the transceiver is no longer part of the SDI II IP core and the TX PLL is separated from the transceiver PHY.

**Figure 1. Triple Rate SDI II with External VCXO Reference Design Block Diagram**

This figure shows a high-level block diagram of the triple rate SDI II VCXO reference design.




*Note:* The Arria 10 Transceiver Native PHY IP core does not provide the SDI triple rate duplex preset option because only RX requires dynamic reconfiguration. Multiple profiles in duplex mode may include some TX registers that are not necessary. The multiple profiles for HD-SDI and 3G-SDI are provided in the SDI triple rate RX preset for dynamic reconfiguration. The Arria 10 Native PHY (RX) IP is added in the Quartus Prime project to include the `*_CFG0.sv` and `**_CFG1.sv` files for the SDI triple rate duplex reconfiguration to function properly.

For more information about each component in the block diagram, refer to Reference Design Components on page 18.

## 1.1.1 Setting up the Hardware for Triple Rate SDI II with External VCXO Reference Design

Complete the steps in the following topics to set up the required hardware for the triple rate SDI II with external VCXO reference design.

### Hardware and Software Requirements

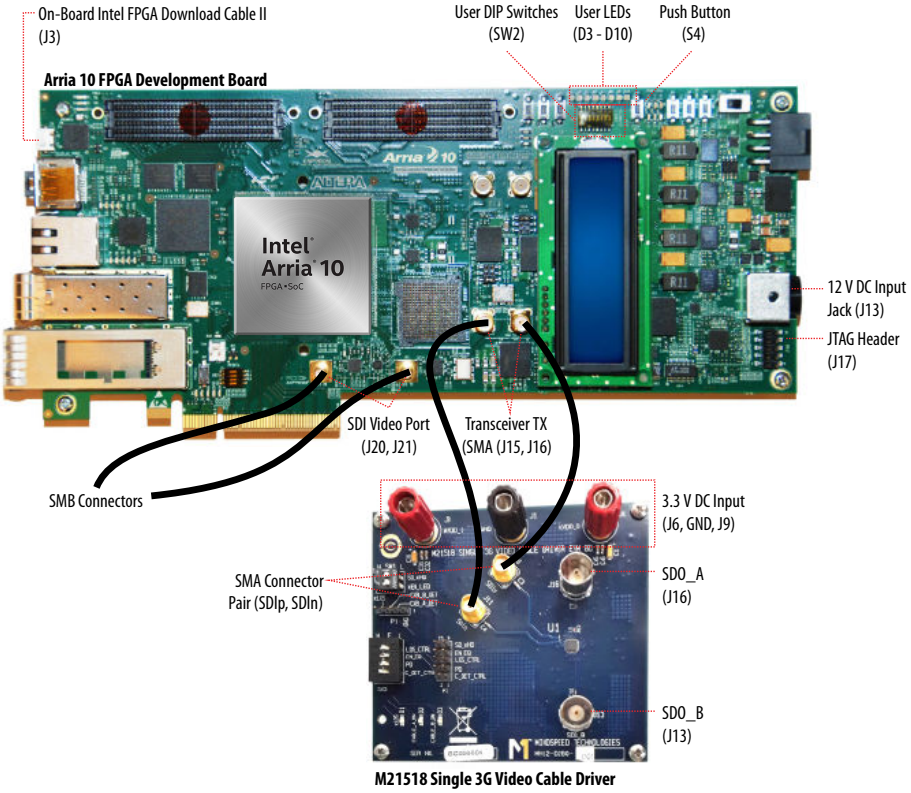
The triple rate SDI II with external VCXO reference design requires the following hardware and software:

- Arria 10 GX FPGA Development Board (10AX115S3F45E2SGE3)
- M21518 Single 3G Video Cable Driver
- SMA cables, BNC plug to SMB plug cables, and BNC cables
- SDI Signal Analyzer
- SDI Signal Generator or Internal Pattern Generator
- Intel® Quartus® Prime software version 16.0

### Connecting the Development Board to the Cable Driver

Connect the J15 and J16 connectors on the Arria 10 GX FPGA development board to the SDIp and SDIn connector pair on the M21518 Single Video 3G cable driver using the SMA cables.

**Figure 2. Hardware Connection**



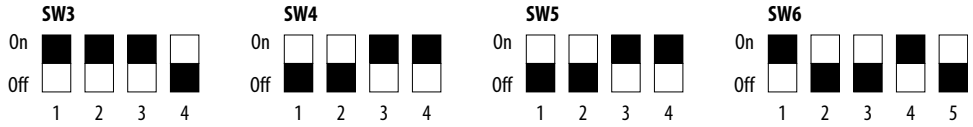
### Setting the DIP Switches

Set the DIP switches of the development board as specified in the following table.

**Table 1. DIP Switch Control Settings**

| DIP Switch | | Schematic Signal Name | Description | Setting |
|---|---|---|---|---|
| SW3 (PCIe*) | 1 | X1 | ON for PCIe X1 | ON |
| | 2 | X4 | ON for PCIe X4 | ON |
| | 3 | X8 | ON for PCIe X8 | ON |
| | 4 | — | OFF for 1.35 V MEM_VDD power rail | OFF |
| SW4 (JTAG) | 1 | Arria 10 | OFF to enable the Arria 10 in the JTAG chain | OFF |
| | 2 | MAX V | OFF to enable the MAX V device in the JTAG chain | OFF |
| | 3 | FMCA | ON to bypass the FMCA connector in the JTAG chain | ON |
| | 4 | FMCB | ON to bypass the FMCB connector in the JTAG chain | ON |
| SW5 (Configuration)[1] | 1 | MSEL0 | ON for MSEL0 = 1; for FPP standard mode | OFF |
| | 2 | MSEL1 | ON for MSEL1 = 0; for FPP standard mode | OFF |
| | 3 | MSEL2 | ON for MSEL2 = 0; for FPP standard mode | ON |
| | 4 | VIDEN | OFF for enabling VID_EN for the Smart Voltage ID (SmartVID) feature | ON |
| SW6 (Board Settings) | 1 | CLK_SEL | ON for 100 MHz on-board clock oscillator selection<br>OFF for SMA input clock selection | ON |
| | 2 | CLK_EN | OFF for setting CLK_ENABLE signal high to the MAX V device | OFF |
| | 3 | Si516_FS | ON for setting the SDI REFCLK frequency to 148.35 MHz<br>OFF for setting the SDI REFCLK frequency to 148.5 MHz | OFF |
| | 4 | FACTORY | ON to load factory image from flash<br>OFF to load user hardware from flash | ON |
| | 5 | RZQ_B2K | ON for setting RZQ resistor of Bank 2K to 99.17 ohm<br>OFF for setting RZQ resistor of Bank 2K to 240 ohm | OFF |

**Figure 3. DIP Switches**




### Connecting the Hardware to the Power Supplies

Connect the following hardware to the respective power supply:

1 Set the MSEL [2:0] bits according to your chosen configuration scheme.

1. The development board to the 12 V DC input (J13) power supply.
2. The J6 and J9 inputs of the M21518 Single Video 3G cable driver to a 3.3 V power supply.
3. The J1 input of the M21518 Single Video 3G cable driver to a GND power supply.

### Port Assignments

When you set up the hardware, the following physical ports are assigned to the SDI channels.

**Table 2. SDI Channels and Ports**

| SDI Channel | Hardware | RX Port | TX Port |
|---|---|---|---|
| 0 | Arria 10 GX development board | SDI_RX_P (J20) | SDI_TX_P (J21) |
| 1 | M21518 single 3G video cable driver | – | SDO_A (J16) |

## 1.1.2 Running the Triple Rate SDI II with External VCXO Reference Design

When the board is set up and the FPGA is configured, you can start running the demonstration tests. Subsequent topics describe the tests that you can run.

### Table 3. DIP Switch

Use the SW2 DIP switches to specify the input and output type for the tests. A logical 0 indicates that the switch is ON; a logical 1 indicates that the switch is OFF.

| SW2 | Description |
|---|---|
| 8 | • 0: 75% color bars<br>• 1: 100% color bars |
| 7 | • 0: Output color bars<br>• 1: Output pathological |
| 6 | • 0: Output color<br>• 1: Output no color |
| 5 | Unused |
| 4:1 | • 0000: SD – 525i59.94<br>• 0001: SD – 625i50<br>• 0010: HD – 1080i60<br>• 0011: HD – 1080i50<br>• 0100: HD – 1080p24<br>• 0101: HD – 720p60<br>• 0110: HD – 720p30<br>• 0111: HD – 1080p30<br>• 1000: HD – 1080p25<br>• 1001: 3Ga – 1080p60<br>• 1010: 3Ga – 1080p50<br>• 1011: 3Gb – 2x1080i60<br>• 1100: 3Gb – 2x720p30<br>• 1101: 3Gb – 2x1080p30<br>• 1110: 3Gb – 1080p60<br>• 1111: 3Gb – 1080p50 |

### Table 4. User LEDs

The User LEDs indicate the expected results. A logical 1 indicates that the LED illuminates, a logical 0 indicates otherwise.

| User LEDs | Description |
|---|---|
| D3 | The heartbeat of the transmitter clock out for channel 0. |
| D4 | The heartbeat of the receiver recovered clock out for channel 0. |
| D5 | Frame locked for channel 0. |
| D6 | TRS locked for channel 0. |
| D7, D8 | RX signal standard for channel 0:<br>• SD: [D7, D8]=00<br>• HD: [D7, D8]=01<br>• 3Ga: [D7, D8]=11<br>• 3Gb: [D7, D8]=10 |
| D9, D10 | Internal pattern generator signal standard for channel 1: |

*continued...*

| User LEDs | Description |
|---|---|
| | • SD: [D9, D10]=00<br>• HD: [D9, D10]=01<br>• 3Ga: [D9, D10]=11<br>• 3Gb: [D9, D10]=10 |

*Note:* You need to compile and configure the design before you run the tests. For more information about compiling and configuring the design, refer to Compiling the Design and Configuring the FPGA on page 22.

### Reset

You may reset the reference design by pressing the S4 push button on the development board.

### 1.1.2.1 Test Pattern Transmitter

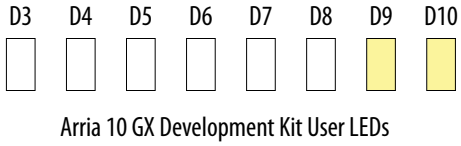
Follow these steps to run the test:

1. Ensure that the J15 and J16 connectors on the Arria 10 GX FPGA development board are connected to the SDIp and SDIn connector pair on the M21518 Single Video 3G cable driver.
2. Connect an SDI signal analyzer to the SDI transmitter output, SDO_A (J16), on the M21518 single video 3G cable driver.
3. Use the SW2 switches to change the input or output type.
4. Check the result on the SDI signal analyzer.

The test demonstrates the following operations:

- Channel 1 generates and transmits the video data from the Transceiver TX SMA connector pair J15 and J16 on the development board to the SMA connector pair SDIp and SDIn on the M21518 single video 3G cable driver.
- The cable driver then transmits the SDI signal at the connector SDO_A (J16).
- The following user LEDs indicate the respective conditions:

**Figure 4. User LEDs**



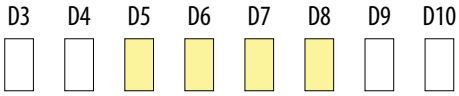
### 1.1.2.2 Receiver

To run the test, connect an SDI signal generator to the receiver input, SDI_RX_P (J20), of channel 0.

This test uses the following user LEDs to indicate the respective conditions:

- D7 and D8 indicate the receiver signal standard.
- D6 illuminates when the trs_locked signal for channel 0 is asserted.
- D5 illuminates when the frame_locked signal for channel 0 is asserted.

**Figure 5. User LEDs**




Arria 10 GX Development Kit User LEDs

### 1.1.2.3 Serial Loopback

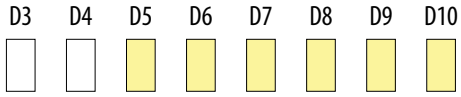
Follow these steps to run the test:

1. Connect the transmitter output, SDO_A (J16), of channel 1 to the receiver input, SDI_RX_P (J20), of channel 0.
2. Use the SW2 switches to change the input or output type.

This test uses the following user LEDs to indicate the respective conditions:

- D9 and D10 indicate the internal pattern generator standard, which transmits through channel 1 of the transmitter.
- D7 and D8 indicate the receiver signal standard.
- D6 illuminates when the `trs_locked` signal for channel 0 is asserted.
- D5 illuminates when the `frame_locked` signal for channel 0 is asserted.

**Figure 6. User LEDs**




Arria 10 GX Development Kit User LEDs

### 1.1.2.4 Parallel Loopback

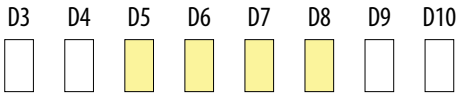
Follow these steps to run the test:

1. Connect an SDI signal generator to the receiver input, SDI_RX_P (J20), of channel 0.
2. Connect an SDI signal analyzer to the transmitter output, SDI_TX_P (J21), of channel 0.
3. Check the result on the SDI signal analyzer.

This test uses the following user LEDs to indicate the respective conditions:

- D7 and D8 indicate the receiver signal standard.
- D6 illuminates when the `trs_locked` signal for channel 0 is asserted.
- D5 illuminates when the `frame_locked` signal for channel 0 is asserted.

**Figure 7. User LEDs**



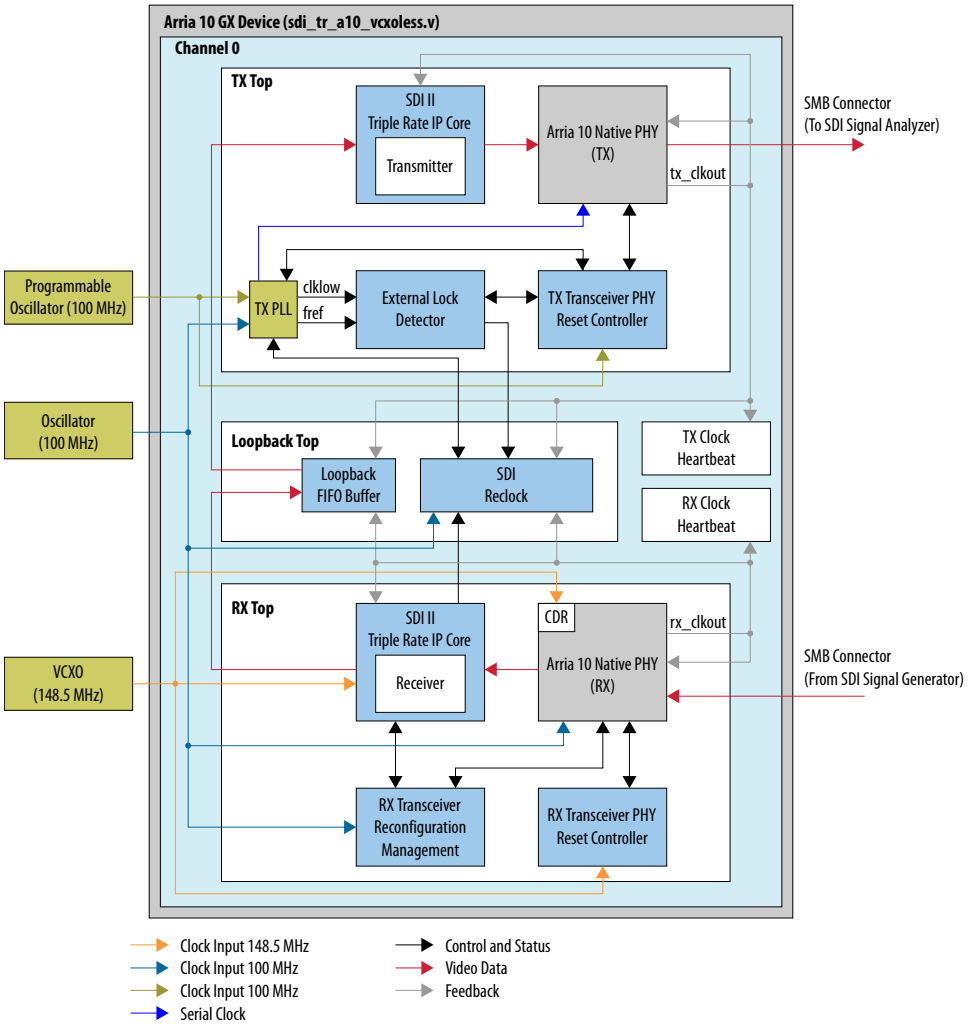

Arria 10 GX Development Kit User LEDs

## 1.2 Triple Rate SDI II VCXO Removal Reference Design

This reference design consists of channel 0—SDI II IP in transmitter and receiver IP cores in simplex mode.

**Figure 8. Triple Rate SDI II VCXO Removal Reference Design Block Diagram**

This figure shows a high-level block diagram of the triple rate SDI II VCXO removal reference design.




For more information about each component in the block diagram, refer to Reference Design Components on page 18.

## 1.2.1 Setting up the Hardware for Triple Rate SDI II VCXO Removal Reference Design

Complete the steps in the following topics to set up the required hardware for triple rate SDI II VCXO removal reference design.

### Hardware and Software Requirements

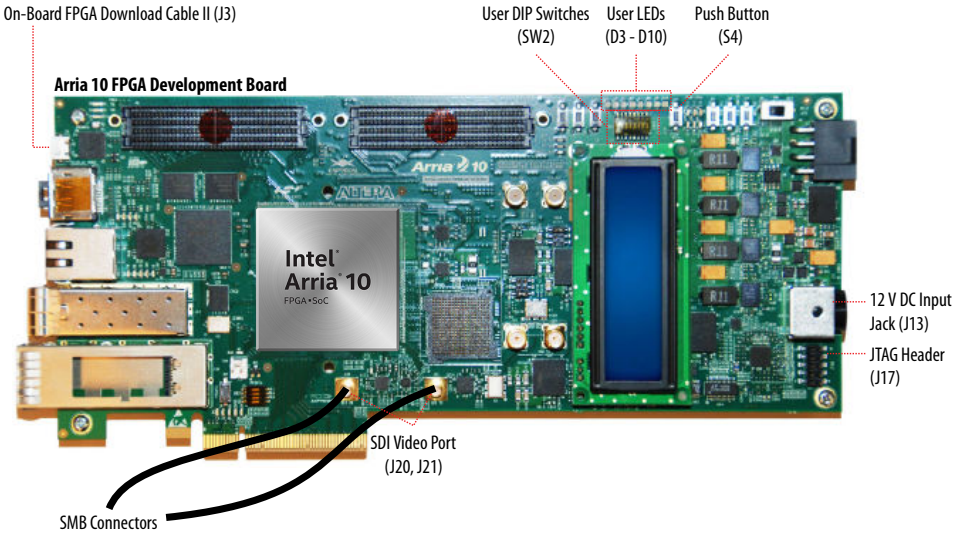
The triple rate SDI II VCXO removal reference design requires the following hardware and software:

- Arria 10 GX FPGA Development Board (10AX115S3F45E2SGE3)
- BNC plug to SMB plug cables
- SDI Signal Analyzer
- SDI Signal Generator
- Quartus Prime version 16.0

### Connecting the Development Board to the Cable Driver

Connect the J20 (RX port) to external video source and the J21 (TX port) to video scope using BNC plug to SMB plug cables.

**Figure 9. Hardware Connection**




### Setting the DIP Switches

Set the DIP switches of the development board as specified in the following table.

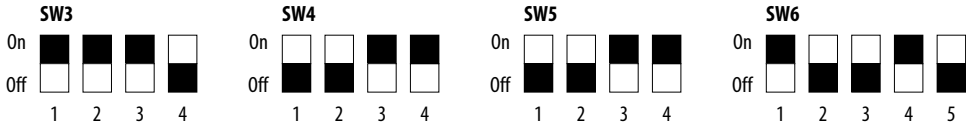
**Table 5. DIP Switch Control Settings**

| DIP Switch | | Schematic Signal Name | Description | Setting |
|---|---|---|---|---|
| SW3 (PCIe) | 1 | X1 | ON for PCIe X1 | ON |
| | 2 | X4 | ON for PCIe X4 | ON |
| | 3 | X8 | ON for PCIe X8 | ON |
| | 4 | — | OFF for 1.35 V MEM_VDD power rail | OFF |
| SW4 (JTAG) | 1 | Arria 10 | OFF to enable the Arria 10 in the JTAG chain | OFF |
| | 2 | MAX V | OFF to enable the MAX V device in the JTAG chain | OFF |

*continued...*

| DIP Switch | | Schematic Signal Name | Description | Setting |
|---|---|---|---|---|
| | 3 | FMCA | ON to bypass the FMCA connector in the JTAG chain | ON |
| | 4 | FMCB | ON to bypass the FMCB connector in the JTAG chain | ON |
| SW5 (Configuration)[2] | 1 | MSEL0 | ON for MSEL0 = 1; for FPP standard mode | OFF |
| | 2 | MSEL1 | ON for MSEL1 = 0; for FPP standard mode | OFF |
| | 3 | MSEL2 | ON for MSEL2 = 0; for FPP standard mode | ON |
| | 4 | VIDEN | OFF for enabling VID_EN for the Smart Voltage ID (SmartVID) feature | ON |
| SW6 (Board Settings) | 1 | CLK_SEL | ON for 100 MHz on-board clock oscillator selection<br>OFF for SMA input clock selection | ON |
| | 2 | CLK_EN | OFF for setting CLK_ENABLE signal high to the MAX V device | OFF |
| | 3 | Si516_FS | ON for setting the SDI REFCLK frequency to 148.35 MHz<br>OFF for setting the SDI REFCLK frequency to 148.5 MHz | OFF |
| | 4 | FACTORY | ON to load factory image from flash<br>OFF to load user hardware from flash | ON |
| | 5 | RZQ_B2K | ON for setting RZQ resistor of Bank 2K to 99.17 ohm<br>OFF for setting RZQ resistor of Bank 2K to 240 ohm | OFF |

**Figure 10. DIP Switches**




### Connecting the Hardware to the Power Supplies

Connect the development board to the 12V DC input (J13) power supply.

### Port Assignments

When you set up the hardware, the following physical ports are assigned to the SDI channels.

**Table 6. SDI Channels and Ports**

| SDI Channel | Hardware | RX Port | TX Port |
|---|---|---|---|
| 0 | Arria 10 GX development board | SDI_RX_P (J20) | SDI_TX_P (J21) |

2 Set the MSEL [2:0] bits according to your chosen configuration scheme.

## 1.2.2 Running the SDI II VCXO Removal Reference Design

When the board is set up and the FPGA is configured, you can start running the demonstration tests. Subsequent topics describe the tests that you can run.

**Table 7. User LEDs**

The User LEDs indicate the expected results. A logical 1 indicates that the LED illuminates, a logical 0 indicates otherwise.

| User LEDs | Description |
|---|---|
| D3 | The heartbeat of the transmitter clock out for channel 0. |
| D4 | The heartbeat of the receiver recovered clock out for channel 0. |
| D5 | Frame locked for channel 0. |
| D6 | TRS locked for channel 0. |
| D7 | Alignment locked for channel 0. |
| D8, D9, D10 | RX signal standard for channel 0:<br>• SD: [D8, D9, D10]=000<br>• HD: [D8, D9, D10]=001<br>• 3Ga: [D8, D9, D10]=011<br>• 3Gb: [D8, D9, D10]=010 |

*Note:* You need to compile and configure the design before you run the tests. For more information about compiling and configuring the design, refer to Compiling the Design and Configuring the FPGA on page 22.

### Reset

You may reset the reference design by pressing the S4 push button on the development board.

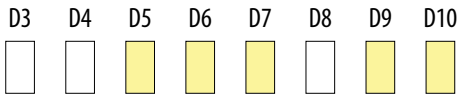
### 1.2.2.1 Receiver

To run the test, connect an SDI signal generator to the receiver input, SDI_RX_P (J20), of channel 0.

This test uses the following user LEDs to indicate the respective conditions:

- D8, D9 and D10 indicate the receiver signal standard.
- D7 illuminates when the `align_locked` signal for channel 0 is asserted.
- D6 illuminates when the `trs_locked` signal for channel 0 is asserted.
- D5 illuminates when the `frame_locked` signal for channel 0 is asserted.

**Figure 11. User LEDs**




Arria 10 GX Development Kit User LEDs

### 1.2.2.2 Parallel Loopback

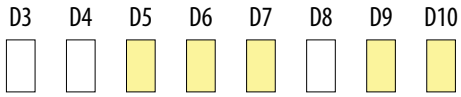
To run the parallel loopback demonstration:

1. Connect an SDI signal generator to the channel 0 receiver input of SDI_RX_P (J20).
2. Connect an SDI signal analyzer to the channel 0 transmitter output of SDI_TX_P (J21).
3. Check the result on the SDI signal analyzer.

This test uses the following user LEDs to indicate the respective conditions:

- D8, D9 and D10 indicate the receiver signal standard.
- D7 illuminates when the align_locked signal for channel 0 is asserted.
- D6 illuminates when the trs_locked signal for channel 0 is asserted.
- D5 illuminates when the frame_locked signal for channel 0 is asserted.

**Figure 12. User LEDs**




Arria 10 GX Development Kit User LEDs

## 1.3 Reference Design Components

The following table describes each component in the reference designs.

**Table 8. Design Components Specific to Triple Rate SDI II with External VCXO Reference Design**

| | |
|---|---|
| Triple-rate SDI II IP Core | The SDI II IP core.<br>• Channel 0—the instance of the SDI II IP in this channel is configured to support full-duplex operations and the triple-rate video standards, SD-SDI, HD-SDI, and 3G-SDI.<br>The SDI II receiver, TX PLL, and TX transceiver PHY reset controller use the 148.5 Mhz/148.35 Mhz external clock source from the VCXO (si516) block on the development board. The RX data is looped back to the transmitter through a FIFO buffer. The interface is configured to operate at 270 Mbps, 1.485/1.4835 Gbps, or 2.97/2.967 Gbps.<br>• Channel 1—the instance of the SDI II IP is configured as a transmitter that supports the triple-rate video standards, SD-SDI, HD-SDI, and 3G-SDI. This instance acts as a video source, and transmits video stream at 270 Mbps (SD), 1.485/1.4835 Gbps (HD), or 2.97/2.967 Gbps (3G) through the transceiver TX pins. The video pattern generator provides the input to this instance. |
| TX PLL | The Arria 10 fPLL and Arria 10 Transceiver CMU PLL IP cores. The Arria 10 reference design version 16.0 uses one CMU and one fPLL core as the TX PLL for the Arria 10 Transceiver Native PHY IP core. |

continued...

| | |
|---|---|
| | These IP cores use 148.5/148.35 MHz from external VCXO as a reference clock frequency for channel 0 TX PLL and default 270 MHz from Si5338 Programmable Oscillator as a reference clock frequency for channel 1 TX PLL. |
| Phase Frequency Detector | The phase frequency detector (PFD) block controls the external clock source from the VCXO (si516) block on the development board to minimize the difference in PPM between the data rates of the receiver and transmitter. This control is required to prevent data overflow or underflow. |
| Pattern Generator | The video pattern generator produces the color bar or pathological test patterns. The color bar can be configured as 100% or 75% amplitude. The color bar pattern is the preferred pattern for image generation while the pathological pattern can be used to stress the PLL and cable equalizer of attached video equipment. This video pattern generator can be configured to output various video formats at SD/HD/3G rates. |
| TX/RX Clock Heartbeat | A simple logic to generate a slow clock and display on the LEDs. |

## Table 9. Design Components Specific to Triple Rate SDI II VCXO Removal Reference Design

| | |
|---|---|
| Triple-rate SDI II IP Core | The SDI II IO core.<br>Channel 0—the instance of the SDI II IP in this channel is configured in simplex mode and support SD-SDI, HD-SDI, and 3G-SDI.<br>This channel demonstrates a receiver-to-transmitter loopback by decoding, buffering and retransmitting the received data to be displayed on video scope. The received data comes from an external signal generator.<br>The SDI II receiver uses an external clock 148.5 Mhz. A SDI reclocking soft logic is to retune the fPLL output clock. The generated low jitter output clock (148.5 or 148.35 MHz) of the fPLL is directly supplied to the transceiver input clock. |
| TX PLL | The Arria 10 fPLL IP core.<br>This reference design uses an fPLL core as the TX PLL for the Arria 10 Transceiver Native PHY IP core. It uses default 100 MHz from Si5338 Programmable Oscillator as the reference clock frequency for TX PLL. |
| TX/RX Clock Heartbeat | A simple logic to generate a slow clock and display on the LEDs. |
| SDI Reclock | This block contains a reclock control logic to retune the fPLL output clock to serve as a functional replacement for external VCXO. For more information, refer to SDI Reclock on page 20. |
| External Lock Detector | A soft encrypted IP logic to provide a reliable lock detection of the fPLL. |

## Table 10. Common Design Components

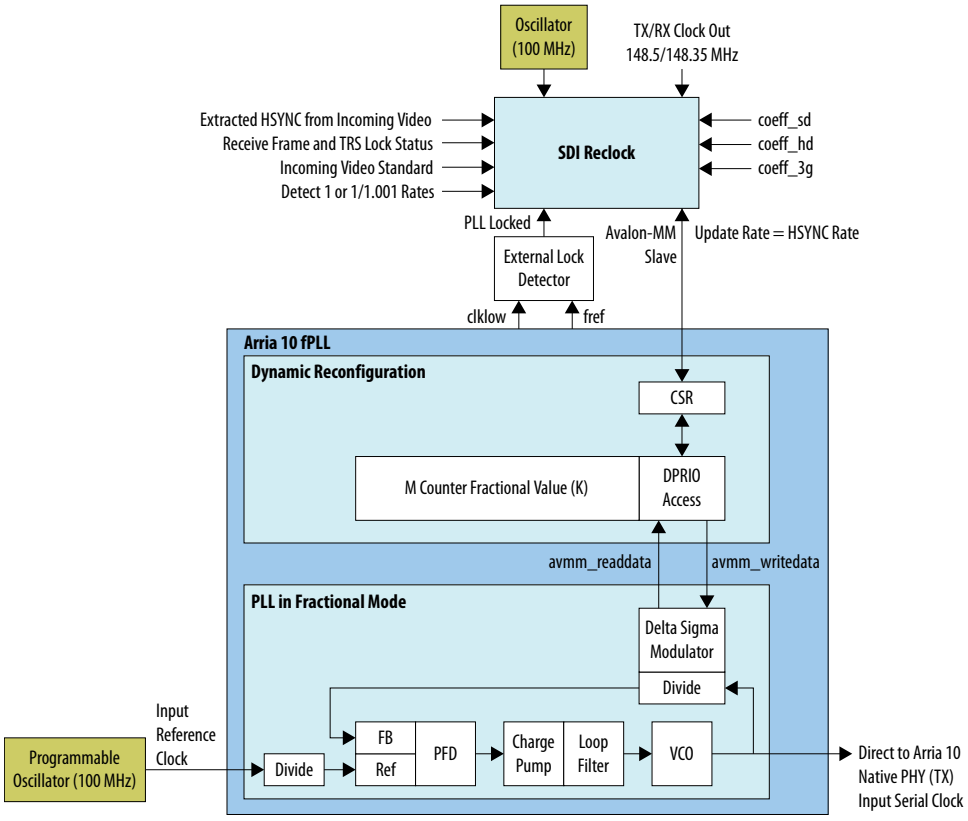
| Name | Description |
|---|---|
| Arria 10 Transceiver Native PHY | The Arria 10 Transceiver Native PHY IP core. The reference design uses this PHY IP core to configure the transceiver PHY for the SDI II protocol implementation. You can select the preset settings for the PHY IP core defined for the SDI II protocol. To apply a preset to the PHY IP core, double click the preset name. When you apply a preset, the PHY parameters are set accordingly for the instance. For example, selecting the **SDI 3G PAL preset** enables all parameters and ports for the 3G- |

*continued...*

| Name | Description |
|---|---|
| | SDI single rate (TX and RX) and triple rate TX with the data rate factor of 1/1 and configured in duplex mode. You may change the direction based on your design needs. |
| TX/RX Transceiver PHY Reset Controller | The Transceiver PHY Reset Controller IP core. This reset controller handles the sequencing of the transceiver reset. Depending on the status received from the transceiver PHY, TX PLL, or the reset input, the reset controller generates the TX or RX reset signals to the transceiver PHY and TX PLL. |
| Loopback FIFO Buffer | This block contains a dual-clock FIFO (DCFIFO) buffer to handle the data transmission across asynchronous clock domains—the receiver recovered clock and transmitter clock out. The receiver sends the decoded RX data to the transmitter through this FIFO buffer. When the receiver is locked, the RX data is written to the FIFO buffer. The transmitter starts reading, encoding, and transmitting the data when half of the FIFO buffer is filled. |
| RX Transceiver Reconfiguration Management | This block contains a state machine that performs the transceiver reconfiguration process. The Avalon-MM reconfiguration interface of this block is connected to the Arria 10 Transceiver Native PHY for the reconfiguration of the SDI II IP core. Although this block supports both TX and RX reconfiguration, this reference design only implements the RX reconfiguration. |

### 1.3.1 SDI Reclock

**Figure 13. SDI Reclock Block Diagram**



The SDI reclock control logic configures the counter settings to adjust the fPLL output clock in real time without reconfiguring the entire FPGA device. In an environment without an external VCXO, the PLL reconfiguration controller needs to configure only the M counter fractional value (K or Mfrac) for the delta-sigma modulator.

The Arria 10 fPLL has a delta sigma fPLL architecture that allows integer and fraction multiplications for the output frequency. The delta-sigma modulator shifts the fractional noise to high frequencies and the PLL filters out the noise. The fPLL uses divide counters and different VCO taps to perform frequency synthesis and phase shift. You need an external lock detection IP logic for a reliable lock detection of the fPLL when it is operating in SDI direct mode.

The reclock control logic generates the Mfrac value during runtime based on the incoming reference signals: horizontal sync value pulse (HSYNC), frame lock status, TRS lock status, incoming video standard, and `rx_clkout_is_ntsc_paln`. The HSYNC signal is extracted from the incoming video stream and the feedback signal, which is the divided value of the TX and RX clock out.

For more details, refer to the reclock source codes in the reference design.

### Related Links

- SDI II IP Core User Guide
  Provides detailed description on the SDI II IP Core.
- Intel Arria 10 Transceiver PHY IP Core User Guide
  Provides detailed description on the Arria 10 Transceiver PHY IP Cores.

## 1.4 Compiling the Design and Configuring the FPGA

You must compile the design before you can configure the FPGA. Because the design is volatile, you must reload the design each time you power on the board.

Follow these steps to compile the design and configure the Arria 10 device:

1. To test the reference designs targeted on Arria 10 device, download the reference design file to your local project directory:
   - Triple Rate SDI II with External VCXO reference design: `sdi_tr_a10_es3_vcxo_an746.par`
   - Triple Rate SDI II VCXO Removal reference design:`sdi_tr_a10_es3_vcxoless_an746.par`
2. Launch the Quartus Prime software.
3. On the File menu, click **New Project Wizard**.
4. On the **New Project Wizard** page, open **Design Template Installation**. Select the design template you want to install. Click Next, then Finish.
5. On the Processing menu, click **Start Compilation**.
6. Before you begin the FPGA configuration, ensure that the Quartus Prime Programmer and the Intel FPGA Download Cable II driver are installed on the host computer, the board is powered, and no other applications that use the JTAG chain are running.
7. Connect the USB cable to the board.
8. On the Tools menu, click **Programmer**.
9. Click **Auto Detect** to display the devices in the JTAG chain and select a device.
10. Right click and select **Change File**. Then, select the appropriate `.sof` file from the project directory and click **Open**.
    - Triple Rate SDI II with External VCXO reference design: `sdi_tr_a10_vcxo.sof`
    - Triple Rate SDI II VCXO Removal reference design: `sdi_tr_a10_vcxoless.sof`
11. Turn on the **Program/Configure** option for the `.sof` file.
12. Click **Start** to download the `.sof` file to the FPGA. Configuration is complete when the progress bar reaches 100%.

## 1.5 Document Revision History

| Date | Version | Changes |
|---|---|---|
| May 2017 | 2017.05.08 | Rebranded as Intel. |
| June 2016 | 2016.06.01 | • Removed the existing Triple Rate SDI II with External VCXO reference design version 15.0.<br>• Added new reference designs for Quartus Prime version 16.0:<br>— Triple Rate SDI II with External VCXO reference design<br>— Triple Rate SDI II VCXO Removal reference design<br>• Updated the PFD codes for external VCXO design.<br>• Update the switch settings. |
| August 2015 | 2015.08.31 | Updated the document structure. |
| June 2015 | 2015.06.29 | Initial release. |