



AN 768: Multi-Rate (Up to 12G) SDI II Reference Design for Intel® Arria® 10 Devices

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1 AN 768: Multi-Rate (Up to 12G) SDI II Reference Design for Intel Arria 10 Devices

The multi rate (up to 12G) Serial Digital Interface II (SDI II) with external voltage-controlled crystal oscillator (VCXO) reference design demonstrates the transmission and reception of video data using the Intel SDI II IP core, Intel Arria® 10 GX FPGA Development Kit, and the Nextera FMC daughter card.

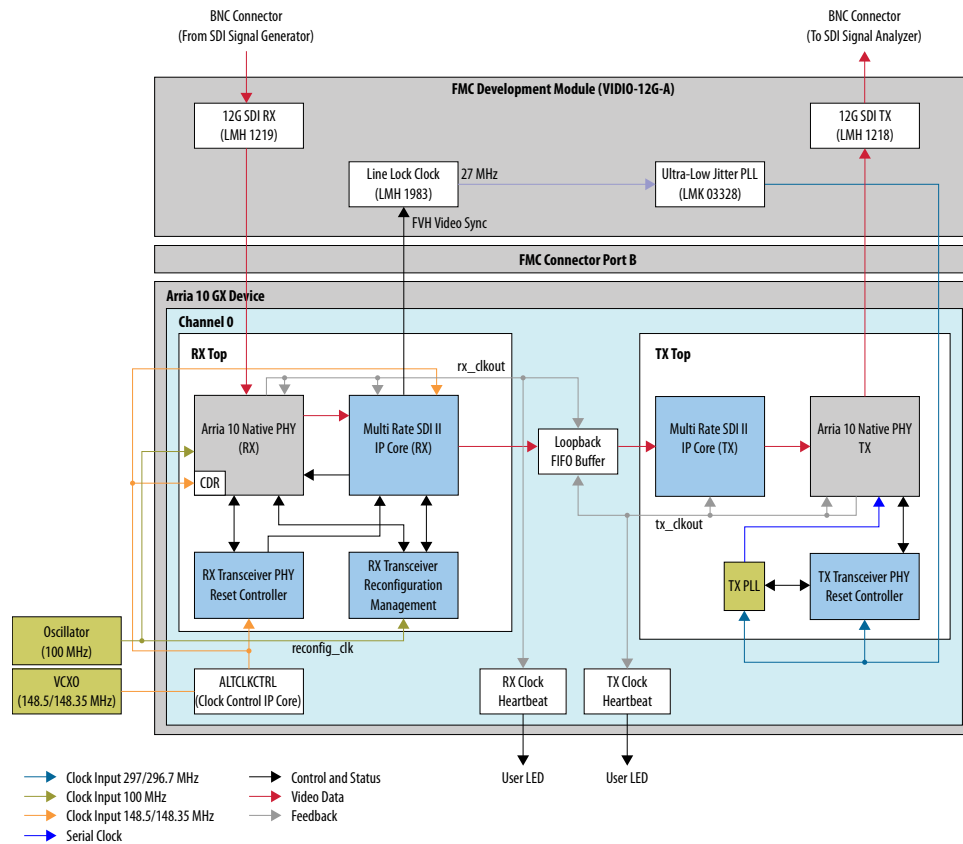
The reference design allows single-link transmission of SDI video data at data rates up to 12 Gbps, which supports 4Kp60. This reference design supports these standards:

- SD-SDI
- HD-SDI
- 3G-SDI
- 6G-SDI
- 12G-SDI

The multi rate SDI II with external VCXO reference design consists of a simplex TX channel and a simplex RX channel. Each channel has its own blocks to operate independently.

- Channel 0 TX
 - Transceiver Native PHY in TX Simplex mode
 - SDI II transmitter instance
 - TX channel Transceiver PHY reset controller
 - TX PLL
- Channel 0 RX
 - Transceiver Native PHY in RX Simplex mode
 - SDI II IP receiver instance
 - RX channel Transceiver PHY reset controller
 - Transceiver reconfiguration management block

Figure 1. Multi Rate (Up to 12G) SDI II with External VCXO Reference Design Block Diagram



For more information about each component in the block diagram, refer to [Reference Design Components](#) on page 9.

Related Links

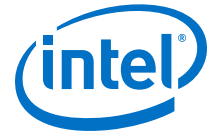
- [Arria 10 Multi Rate \(Up to 12G\) SDI II with External VCXO Reference Design 16.0](#)
Provides the design files for this reference design.
- [SDI II User Guide](#)
- [Arria 10 Transceiver PHY User Guide](#)

1.1 Setting up the Hardware

Complete the steps in the following topics to set up the hardware for the multi rate SDI II with external VCXO reference design.

Hardware and Software Requirements

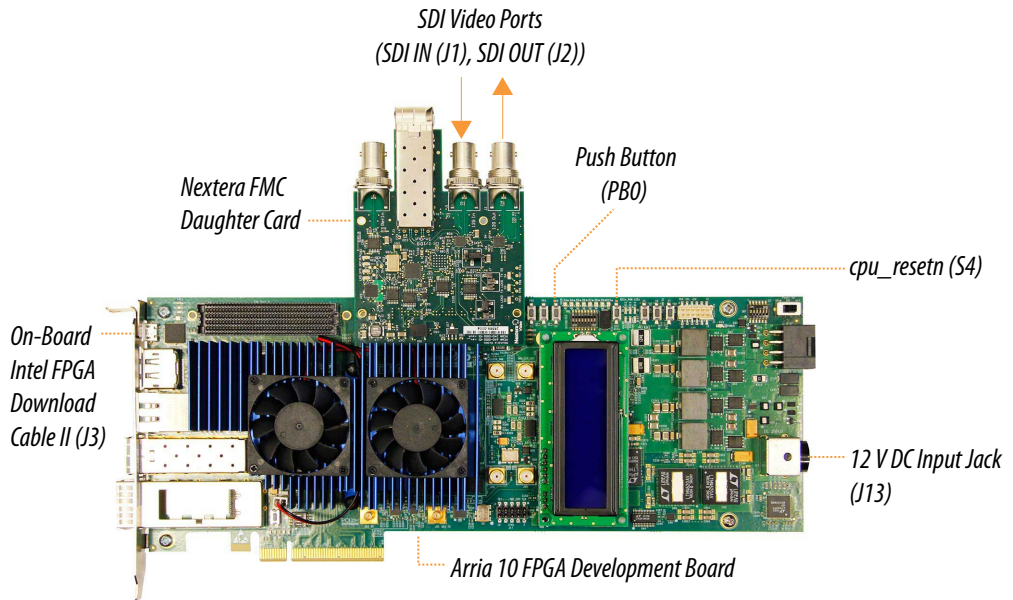
The multi rate SDI II with external VCXO reference design requires the following hardware and software:



- Arria 10 GX FPGA Development Board (10AX115S3F45E2SGE3)
- VIDIO™ FMC Development Module VIDIO-12G-A (Nextera FMC daughter card)
- BNC plug to BNC plug cables
- 12G SDI Signal Analyzer
- 12G SDI Signal Generator
- Quartus® Prime software version 16.0

Connecting the Hardware

Figure 2. Hardware Setup



Plug the Nextera FMC daughter card to the FMC connector port B. Connect the development board to 12V DC input (J13) power supply.

Setting the DIP Switches

Set the DIP switches of the development board as specified below.

Table 1. DIP Switch Control Settings

DIP Switch		Schematic Signal Name	Description	Setting
SW3 (PCIe*)	1	X1	ON for PCIe X1	ON
	2	X4	ON for PCIe X4	ON
	3	X8	ON for PCIe X8	ON
	4	—	OFF for 1.35 V MEM_VDD power rail	OFF
SW4 (JTAG)	1	Arria 10	OFF to enable the Arria 10 device in the JTAG chain	OFF
	2	MAX V	OFF to enable the MAX V device in the JTAG chain	OFF

continued...

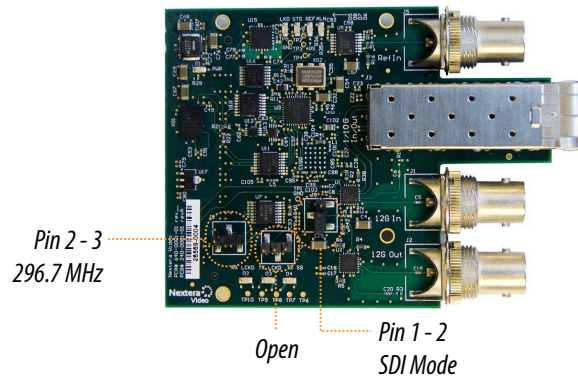
DIP Switch	Schematic Signal Name	Description	Setting		
	3	FMCA	ON to bypass the FMCA connector in the JTAG chain	ON	
	4	FMCB	ON to bypass the FMCB connector in the JTAG chain	ON	
	SW5 (Configuration) ¹	1	MSEL0	ON for MSEL0 = 1; for FPP standard mode	OFF
		2	MSEL1	ON for MSEL1 = 0; for FPP standard mode	OFF
3		MSEL2	ON for MSEL2 = 0; for FPP standard mode	ON	
4		VIDEN	OFF for enabling VID_EN for the Smart Voltage ID (SmartVID) feature	ON	
SW6 (Board Settings)	1	CLK_SEL	ON for 100 MHz on-board clock oscillator selection OFF for SMA input clock selection	ON	
	2	CLK_EN	OFF for setting CLK_ENABLE signal high to the MAX V device	OFF	
	3	Si516_FS	ON for setting the SDI REFCLK frequency to 148.35 MHz OFF for setting the SDI REFCLK frequency to 148.5 MHz	OFF	
	4	FACTORY	ON to load factory image from flash OFF to load user hardware from flash	ON	
	5	RZQ_B2K	ON for setting RZQ resistor of Bank 2K to 99.17 ohm OFF for setting RZQ resistor of Bank 2K to 240 ohm	OFF	

Figure 3. DIP Switches



Jumper Settings

Figure 4. Jumper Settings on the Nextera FMC Daughter Card



- 1 Set the MSEL [2:0] bits according to your chosen configuration scheme.



Note: Refer to the jumper settings to change the jumper (J8) position before you switch between PAL and NTSC video format. You must press the push button (PB0) to trigger a device (LMK03328) power cycling through the PDN pin every time you change the jumper (J8) position.

Table 2. Jumper Settings

Set the jumper position of the Nextera daughter card as specified below.

Jumper Block	Description	Setting
J7	Programming header.	
J8	To switch frequency between PAL and NTSC for TX channel. <ul style="list-style-type: none"> Pin 1-2 = 297 MHz Pin 2-3 = 297/1.001 MHz 	<ul style="list-style-type: none"> 1-2 for PAL 2-3 for NTSC
J9	To select SDI or IP mode. Pin 1-2 =SDI Mode; pin 2-3=IP mode <ul style="list-style-type: none"> Pin 1-2 = SDI Mode Pin 2-3 = IP mode 	1-2

Port Assignments

Table 3. SDI Channels and Ports

FPGA pins and physical ports for SDI TX/RX channels

Transceiver Channel	FPGA Pin	Physical Port on Nextera Daughter Card
Channel 0 TX	AB1/AB2	SDI_OUT (J2)
Channel 0 RX	Y5/Y6	SDI_IN (J1)

Clock Input

Table 4. Input Clock Frequency and FPGA Pins

Input clock frequency and FPGA pins for the multi rate SDI II reference design.

Hardware	Input Clock Frequency	FPGA Input Pin	Description
Arria 10 GX development board	100 MHz	F23/G23	As the channel 0 reconfig clock
Arria 10 GX development board	148.5/148.35 MHz	L37/L38	As the reference clock for channel 0 rx_coreclk and rx_cdr_refclk0, and RX PHY reset controller.
Nextera FMC daughter card	297/296.7 MHz	W8/W7	As the reference clock for channel 0 fPLL, and TX PHY reset controller

1.2 Running the Multi Rate (Up to 12G) SDI II with External VCXO Reference Design

When the board is set up and the FPGA is configured, you can start running the demonstration tests. Subsequent topics describe the tests that you can run.

Table 5. User LEDs

The User LEDs indicate the expected results. A logical 1 indicates that the LED illuminates, a logical 0 indicates otherwise.



User LEDs	Description
D3	The heartbeat of the transmitter clock out for channel 0.
D4	The heartbeat of the receiver recovered clock out for channel 0.
D5	Frame locked for channel 0.
D6	TRS locked for channel 0.
D7	CRC error on Chroma/Luma for channel 0. Applicable for all modes except SD-SDI.
D8-D10	RX signal standard for channel 0: <ul style="list-style-type: none">• SD: [D8, D9, D10] = 000• HD: [D8, D9, D10] = 001• 3Gb: [D8, D9, D10] = 010• 3Ga: [D8, D9, D10] = 011• 6Gb: [D8, D9, D10] = 100• 6Ga: [D8, D9, D10] = 101• 12Gb: [D8, D9, D10] = 110• 12Ga: [D8, D9, D10] = 111

Note: You need to compile and configure the design before you run the tests. For more information about compiling and configuring the design, refer to [Compiling the Design and Configuring the FPGA](#) on page 11.

Reset

You may reset the reference design by pressing the S4 push button on the development board.

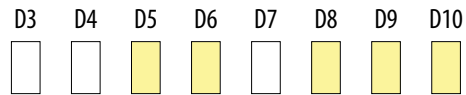
1.2.1 Receiver

To run the test, connect an SDI signal generator to the receiver input, `SDI_IN (J1)`, of channel 0.

This test uses the following user LEDs to indicate the respective conditions:

- D8, D9, and D10 indicate the receiver signal standard.
- D7 illuminates when the CRC error signal for channel 0 is asserted.
- D6 illuminates when the `trs_locked` signal for channel 0 is asserted.
- D5 illuminates when the `frame_locked` signal for channel 0 is asserted.

Figure 5. User LEDs



Arria 10 GX Development Kit User LEDs

1.2.2 Parallel Loopback

Follow these steps to run the parallel loopback test:

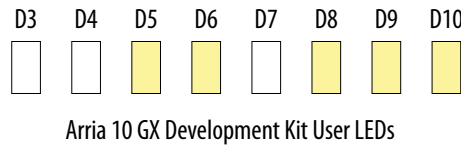


1. Connect an SDI signal generator to the receiver input, SDI_IN (J1), of channel 0.
2. Connect an SDI signal analyzer to the transmitter output, SDI_OUT (J2), of channel 0.
3. Check the result on the SDI signal analyzer.

This test uses the following user LEDs to indicate the respective conditions:

- D8, D9, and D10 indicate the receiver signal standard.
- D7 illuminates when the CRC error signal for channel 0 is asserted.
- D6 illuminates when the trs_locked signal for channel 0 is asserted.
- D5 illuminates when the frame_locked signal for channel 0 is asserted.

Figure 6. User LEDs



Note: LMH1983 does not support 1080 p48 format. For more details, refer to the *Texas Instrument LMH1983 Datasheet*.

1.3 Reference Design Components

The following table describes each component for the multi rate SDI II with external VCXO reference design.

Table 6. Design Components Specific to Multi Rate SDI II with External VCXO Reference Design

TX/RX Multi Rate SDI II IP Core	The SDI II IP core. Channel 0 TX/RX—the instance of the SDI II IP in this channel is configured in simplex TX/RX mode to support SD-SDI, HD-SDI, 3G-SDI, 6G-SDI, and 12G-SDI. Channel 0 of the SDI RX receives external SDI video data from the BNC port through the transceiver RX pin. For more information, refer to Channel Data Rate on page 10.
TX PLL	The Arria 10 fPLL IP core. This reference design uses an fPLL core as the TX PLL for the Arria 10 Transceiver Native PHY IP. This IP core uses 297/296.7 MHz frequency derived from the Nextera FMC daughter card as a reference clock.
TX/RX Arria 10 Transceiver Native PHY	The Altera Arria 10 Transceiver Native PHY IP core. The reference design uses this PHY IP to configure the transceiver PHY for the SDI II protocol implementation. You can select the preset settings for the PHY IP core defined for the SDI II protocol. To apply a preset to the PHY IP core, double click the preset name. When you apply a preset, the PHY parameters are set accordingly for the instance. For example:

continued...



	<ul style="list-style-type: none"> • Selecting the SDI Multi rate (up to 12G-SDI) RX preset enables all parameters and ports for multi rate up to 12G-SDI (RX). This preset contains multiple profiles for HD-SDI, 3G-SDI, 6G-SDI, and 12G-SDI for dynamic reconfiguration. • Selecting the SDI Multi rate (up to 12G-SDI) TX preset enables all the parameters and ports for multi rate up to 12G-SDI (TX) that configures the data rate of 11,880 Mbps or change the data rate to 11,868 Mbps to transmit with data rate factor of 1/1.001
TX/RX Transceiver PHY Reset Controller	The Altera Transceiver PHY Reset Controller IP core. This reset controller handles the sequencing of the transceiver reset. Depending on the status received from the TX transceiver PHY, TX PLL, TX reset input, or the RX transceiver PHY or the SDI asynchronous reset output signal, the reset controller generates the TX or RX reset signals to the TX/RX transceiver PHY, SDI, and TX PLL.
Loopback FIFO Buffer	This block contains a dual-clock FIFO (DCFIFO) buffer to handle the data transmission across asynchronous clock domains—the receiver recovered clock and transmitter clock out. The receiver sends the decoded RX data to the transmitter through this FIFO buffer. When the receiver is locked, the RX data is written to the FIFO buffer. The transmitter starts reading, encoding, and transmitting the data when half of the FIFO buffer is filled.
RX Transceiver Reconfiguration Management	This block contains a state machine that performs the transceiver reconfiguration process. The Avalon-MM reconfiguration interface of this block is connected to the Arria 10 Transceiver Native PHY for the reconfiguration of the SDI II IP core. Although this block supports both TX and RX reconfiguration, this reference design only implements RX reconfiguration.
TX/RX Clock Heartbeat	A simple logic to generate a slow clock and display on the LEDs.
Clock Control IP Core (ALTCLKCTRL)	A clock buffer that promotes <code>refclk_sdi_p</code> to the regional clock.

1.3.1 Channel Data Rate

Based on the input detected by the video standard, this reference design reconfigures the RX transceiver channel's data rate and personal communications system (PCS) data width.

Table 7. RX Transceiver Channel Data Rate and PCS Data Width

Video Standard	PCS-PLD Data Width	Transceiver Data Rate (Gbps)
SD-SDI	20	2.970 ²
HD-SDI	20	1.485 or 1.4835
3G-SDI	20	2.970 or 2.967
6G-SDI	40	5.940 or 5.934
12G-SDI	80	11.880 or 11.868

Based on the standard of the SDI video data received, the SDI II RX core divides the parallel data into one, two, or four 20-bit data streams.

2 11 times oversampling for receiving SD-SDI.

**Table 8. Data Streams for Different Video Standards**

Video Standards	Data Stream
SD-SDI, HD-SDI, 3G-SDI	1
6G-SDI	2
12G-SDI	4

In this reference design, the video data from Channel 0 RX —in four 20-bit data streams —are looped back internally to Channel 0 TX for retransmission.. This channel demonstrates a receiver-to-transmitter loopback by decoding, buffering, and retransmitting the received video data to be displayed on the scope. The SDI II RX core uses an external clock of 148.5 or 148.35 MHz.

Related Links

[TX Sample](#)

Provides more information about TX oversampling.

1.4 Compiling the Design and Configuring the FPGA

You must compile the design before you can configure the FPGA. Because the design is volatile, you must reload the design each time you power on the board.

Follow these steps to compile the design and configure the Arria 10 device:

- To test the reference designs targeted on Arria 10 device, download the reference design file to your local project directory:
Arria 10 Multi Rate (Up to 12G) SDI II with External VCXO Reference Design:
`sdi_mr_a10_vcxo_an768.par`
- Launch the Quartus Prime software.
- On the **File** menu, click **New Project Wizard**.
- On the **New Project Wizard** page, open **Design Template Installation**. Select the design template you want to install. Click **Next**, then **Finish**.
- On the **Processing** menu, click **Start Compilation**.
- Before you begin the FPGA configuration, ensure that the Quartus Prime Programmer and the Intel® FPGA Download Cable II driver are installed on the host computer, the board is powered, and no other applications that use the JTAG chain are running.
- Connect the USB cable to the board.
- On the **Tools** menu, click **Programmer**.
- Click **Auto Detect** to display the devices in the JTAG chain and select a device.
- Right click and select **Change File**. Then, select the appropriate `.sof` file from the project directory and click **Open**.
- Turn on the **Program/Configure** option for the `.sof` file.
- Click **Start** to download the `.sof` file to the FPGA. Configuration is complete when the progress bar reaches 100%.



1.5 Document Revision History

The table shows the revision history for this application note.

Table 9. Document Revision History

Date	Version	Changes
May 2017	2017.05.08	Rebranded as Intel.
June 2016	2016.06.03	Initial release.