Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672
B2	VREFB2N0	GND_PLL3			F5	E4				
B2	VREFB2N0	VCCD_PLL3			E5	H7				
B2	VREFB2N0	GND_PLL3			F6	G7				
B2	VREFB2N0	GND								
B2	VREFB2N0	IO	ASDO	ASDO	C4	E3				
B2	VREFB2N0	IO	nCSO	nCSO	C3	D3				
B2	VREFB2N0	IO	LVDS48p	CRC_ERROR	D3	B2				
B2	VREFB2N0	IO	LVDS48n	CLKUSR	D4	B3				
B2	VREFB2N0	IO	PLL3_OUTp		D5	E5				
B2	VREFB2N0	IO	PLL3_OUTn		D6	F6				
B2	VREFB2N0	VCCIO2								
B2	VREFB2N0	IO	LVDS47p		E3	C2	DQ2L0	DQ1L0		
B2	VREFB2N0	IO	LVDS47n		E4	C3	DQ2L1	DQ1L1		
B2	VREFB2N0	IO	LVDS46p		C1	G5	DQ2L2	DQ1L2		
B2	VREFB2N0	IO	LVDS46n		C2	G6	DQ2L3	DQ1L3		
B2	VREFB2N0	IO	LVDS45p			F3				
B2	VREFB2N0	IO	LVDS45n			F4				
B2	VREFB2N0	IO	LVDS44p			D2				
B2	VREFB2N0	GND								
B2	VREFB2N0	IO	LVDS44n			D1				
B2	VREFB2N0	IO				F7				
B2	VREFB2N0	IO	VREFB2N0		F4	J5				
B2	VREFB2N0	IO	LVDS43p		G6	J8	DQ2L4	DQ1L4		
B2	VREFB2N0	IO	LVDS43n		G5	J7	DQ2L5	DQ1L5		
B2	VREFB2N0	VCCIO2								
B2	VREFB2N0	IO				H6				
B2	VREFB2N0	IO	LVDS42p			E2				
B2	VREFB2N0	IO	LVDS42n			E1				
B2	VREFB2N0	IO	LVDS41p			K6				
B2	VREFB2N0	IO	LVDS41n			K5				
B2	VREFB2N0	IO	LVDS40p			G4				
B2	VREFB2N0	IO	LVDS40n			G3				
B2	VREFB2N0	GND								
B2	VREFB2N0	IO			F3	J6	DQ2L6	DQ1L6	DQ2L0	DQ1L0
B2	VREFB2N0	IO	LVDS39p		D1	K8	DQ2L7	DQ1L7	DQ2L1	DQ1L1
B2	VREFB2N0	IO	LVDS39n		D2	K7		DQ1L8	DQ2L2	DQ1L2

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672
B2	VREFB2N0	IO	LVDS38p		G3	F2	DM2L	DM1L0/BWS#1L0	DQ2L3	DQ1L3
B2	VREFB2N0	IO	LVDS38n		H4	F1	DQ0L0	DQ1L9	DQ2L4	DQ1L4
B2	VREFB2N0	VCCIO2								
B2	VREFB2N0	IO	LVDS37p		H5	G1	CDPCLK0/DQS2L	CDPCLK0/DQS2L	CDPCLK0/DQS2L	CDPCLK0/DQS2L
B2	VREFB2N0	IO	LVDS37n		H6	G2	DQ0L1	DQ1L10		
B2	VREFB2N1	IO	LVDS36p		E1	H3	DQ0L2	DQ1L11	DQ2L5	DQ1L5
B2	VREFB2N1	IO	LVDS36n		E2	H4	DQ0L3	DQ1L12	DQ2L6	DQ1L6
B2	VREFB2N1	IO	LVDS35p		F1	J3	DQ0L4	DQ1L13	DQ2L7	DQ1L7
B2	VREFB2N1	IO	LVDS35n		F2	J4	DQ0L5	DQ1L14		DQ1L8
B2	VREFB2N1	IO	LVDS34p			H2			DM2L	DM1L0/BWS#1L0
B2	VREFB2N1	IO	LVDS34n			H1				
B2	VREFB2N1	GND								
B2	VREFB2N1	IO	LVDS33p			J2				
B2	VREFB2N1	GND								
B2	VREFB2N1	IO	LVDS33n			J1			DQ0L0	DQ1L9
B2	VREFB2N1	IO	LVDS32p			K4			DQ0L1	DQ1L10
B2	VREFB2N1	IO	LVDS32n			K3			DQ0L2	DQ1L11
B2	VREFB2N1	VCCIO2								
B2	VREFB2N1	IO	LVDS31p			K1			DQ0L3	DQ1L12
B2	VREFB2N1	IO	LVDS31n			K2			DQ0L4	DQ1L13
B2	VREFB2N1	IO	VREFB2N1		H3	L4				
B2	VREFB2N1	IO	LVDS30p		G1	N9				
B2	VREFB2N1	IO	LVDS30n		G2	P9				
B2	VREFB2N1	IO	LVDS29p		J6	L7			DQ0L5	DQ1L14
B2	VREFB2N1	IO	LVDS29n		J5	L6			DQ0L6	DQ1L15
B2	VREFB2N1	GND								
B2	VREFB2N1	IO	LVDS28p		H1	L2	DQ0L6	DQ1L15	DQ0L7	DQ1L16
B2	VREFB2N1	IO	LVDS28n		H2	L3	DQ0L7	DQ1L16		DQ1L17
B2	VREFB2N1	VCCIO2								
B2	VREFB2N1	GND								
B2	VREFB2N1	IO	LVDS27p		J3	M4				
B2	VREFB2N1	VCCIO2								
B2	VREFB2N1	IO	LVDS27n		J4	M5		DQ1L17	DM0L	DM1L1/BWS#1L1
B2	VREFB2N1	IO	LVDS26p		J1	M3	DPCLK0/DQS0L	DPCLK0/DQS0L	DPCLK0/DQS0L	DPCLK0/DQS0L
B2	VREFB2N1	IO	LVDS26n		J2	M2				
B2	VREFB2N1	TDI		TDI	K5	M8				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672
B2	VREFB2N1	TCK		TCK	K2	M6				
B2	VREFB2N1	TMS		TMS	K6	L8				
B2	VREFB2N1	TDO		TDO	L5	M7				
B2	VREFB2N1	DCLK	DCLK	DCLK	L6	N6				
B2	VREFB2N1	DATA0	DATA0	DATA0	K4	N3				
B2	VREFB2N1	nCE		nCE	K1	N4				
B2	VREFB2N1	CLK0	LVDSCLK0p/input(3)		L1	N2				
B2	VREFB2N1	CLK1	LVDSCLK0n/input(3)		L2	N1				
B2	VREFB2N1	GND								
B2	VREFB2N1	nCONFIG		nCONFIG	L4	N7				
B1	VREFB1N0	CLK2	LVDSCLK1p/input(3)		M1	P2				
B1	VREFB1N0	CLK3	LVDSCLK1n/input(3)		M2	P1				
B1	VREFB1N0	VCCIO1								
B1	VREFB1N0	IO	LVDS25p		M5	P3	DPCLK1/DQS1L	DPCLK1/DQS1L	DPCLK1/DQS1L	DPCLK1/DQS1L
B1	VREFB1N0	IO	LVDS25n		M6	P4				
B1	VREFB1N0	IO	LVDS24p		N1	R2	DM0L	DM1L1/BWS#1L1	DQ1L0	DQ3L0
B1	VREFB1N0	IO	LVDS24n		N2	R3	DQ1L0	DQ3L0	DQ1L1	DQ3L1
B1	VREFB1N0	GND								
B1	VREFB1N0	IO	LVDS23p		P1	R4	DQ1L1	DQ3L1	DQ1L2	DQ3L2
B1	VREFB1N0	GND								
B1	VREFB1N0	IO	LVDS23n		P2	R5	DQ1L2	DQ3L2		
B1	VREFB1N0	GND								
B1	VREFB1N0	IO	LVDS22p		N6	P7	DQ1L3	DQ3L3	DQ1L3	DQ3L3
B1	VREFB1N0	IO	LVDS22n		N5	P6			DQ1L4	DQ3L4
B1	VREFB1N0	IO	LVDS21p			T2			DQ1L5	DQ3L5
B1	VREFB1N0	IO	LVDS21n			T3			DQ1L6	DQ3L6
B1	VREFB1N0	VCCIO1								
B1	VREFB1N0	IO	LVDS20p		N3	R6	DQ1L4	DQ3L4	DQ1L7	DQ3L7
B1	VREFB1N0	IO	LVDS20n		N4	R7	DQ1L5	DQ3L5	DQ1L8	DQ3L8
B1	VREFB1N0	IO	VREFB1N0		P3	T4				
B1	VREFB1N0	IO	LVDS19p			U2			DM1L/BWS#1L	DM3L0/BWS#3L0
B1	VREFB1N0	IO	LVDS19n			U1				
B1	VREFB1N0	GND								
B1	VREFB1N0	IO	LVDS18p		P5	U3	DQ1L6	DQ3L6		
B1	VREFB1N0	IO	LVDS18n		P6	U4	DQ1L7	DQ3L7		
B1	VREFB1N0	IO	LVDS17p		R1	V1	DQ1L8	DQ3L8		

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672
B1	VREFB1N0	IO	LVDS17n		R2	V2	DM1L/BWS#1L	DM3L0/BWS#3L0		
B1	VREFB1N0	VCCIO1								
B1	VREFB1N0	IO	LVDS16p			T7				
B1	VREFB1N0	IO	LVDS16n			T6				
B1	VREFB1N0	IO	LVDS15p			V4				
B1	VREFB1N0	IO	LVDS15n			V3				
B1	VREFB1N0	IO	LVDS14p		T1	W2			DQ3L0	DQ3L9
B1	VREFB1N0	IO	LVDS14n		T2	W1			DQ3L1	DQ3L10
B1	VREFB1N0	GND								
B1	VREFB1N1	IO	LVDS13p		P4	U6			DQ3L2	DQ3L11
B1	VREFB1N1	IO	LVDS13n		R4	U7			DQ3L3	DQ3L12
B1	VREFB1N1	IO				U5			DQ3L4	DQ3L13
B1	VREFB1N1	IO	LVDS12p		U1	W4	CDPCLK1/DQS3L	CDPCLK1/DQS3L	CDPCLK1/DQS3L	CDPCLK1/DQS3L
B1	VREFB1N1	IO	LVDS12n		U2	W3				
B1	VREFB1N1	VCCIO1								
B1	VREFB1N1	IO	LVDS11p			Y2				
B1	VREFB1N1	IO	LVDS11n			Y1			DQ3L5	DQ3L14
B1	VREFB1N1	IO	LVDS10p		R5	V5	DQ3L0	DQ3L9	DQ3L6	DQ3L15
B1	VREFB1N1	IO	LVDS10n		R6	V6	DQ3L1	DQ3L10	DQ3L7	DQ3L16
B1	VREFB1N1	IO	LVDS9p			AA2			DQ3L8	DQ3L17
B1	VREFB1N1	GND								
B1	VREFB1N1	IO	LVDS9n			AA1			DM3L/BWS#3L	DM3L1/BWS#3L1
B1	VREFB1N1	GND								
B1	VREFB1N1	IO	LVDS8p		V1	Y3	DQ3L2	DQ3L11		
B1	VREFB1N1	IO	LVDS8n		V2	Y4	DQ3L3	DQ3L12		
B1	VREFB1N1	IO	LVDS7p		T5	R8	DQ3L4	DQ3L13		
B1	VREFB1N1	IO	LVDS7n		T6	T8				
B1	VREFB1N1	IO			T3	V7				
B1	VREFB1N1	VCCIO1								
B1	VREFB1N1	IO	VREFB1N1		U3	W6				
B1	VREFB1N1	IO	LVDS6p		W1	AB2	DQ3L5	DQ3L14		
B1	VREFB1N1	IO	LVDS6n		W2	AB1	DQ3L6	DQ3L15		
B1	VREFB1N1	IO	LVDS5p		Y1	AA4	DQ3L7	DQ3L16		
B1	VREFB1N1	IO	LVDS5n		Y2	AA3	DQ3L8	DQ3L17		
B1	VREFB1N1	IO	LVDS4p			AC2				
B1	VREFB1N1	IO	LVDS4n			AC1				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672
B1	VREFB1N1	GND								
B1	VREFB1N1	IO	LVDS3p			AA5				
B1	VREFB1N1	IO	LVDS3n			Y5				
B1	VREFB1N1	IO	LVDS2p		W3	AD2	DM3L/BWS#3L	DM3L1/BWS#3L1		
B1	VREFB1N1	IO	LVDS2n		W4	AD3				
B1	VREFB1N1	IO	LVDS1p			AE2				
B1	VREFB1N1	VCCIO1								
B1	VREFB1N1	IO	LVDS1n			AE3				
B1	VREFB1N1	IO	LVDS0p		Y3	AB3				
B1	VREFB1N1	IO	LVDS0n		Y4	AB4				
B1	VREFB1N1	IO			W5	AC3				
B1	VREFB1N1	IO	PLL1_OUTp		U4	AA7				
B1	VREFB1N1	IO	PLL1_OUTn		V4	AA6				
B1	VREFB1N1	GND								
B1	VREFB1N1	GND_PLL1			U5	W7				
B1	VREFB1N1	VCCD_PLL1			U6	Y7				
B1	VREFB1N1	GND_PLL1			V5	Y6				
B8	VREFB8N1	VCCA_PLL1			U7	AA8				
B8	VREFB8N1	GNDA_PLL1			V7	Y8				
B8	VREFB8N1	GND								
B8	VREFB8N1	IO	LVDS188n	DEV_OE	AA3	AE4				
B8	VREFB8N1	IO	LVDS188p		AB3	AF4			DM1B	
B8	VREFB8N1	IO	LVDS187p		AB4	AC5			DQ1B7	
B8	VREFB8N1	IO	LVDS187n		AA4	AC6			DQ1B6	
B8	VREFB8N1	IO	LVDS186p		Y5	AD4			DQ1B5	
B8	VREFB8N1	IO	LVDS186n		Y6	AD5	DM3B/BWS#3B	DM3B1/BWS#3B1	DQ1B4	
B8	VREFB8N1	VCCIO8								
B8	VREFB8N1	IO	LVDS185p		AB5	AE5	CDPCLK2/DQS1B	CDPCLK2/DQS1B	CDPCLK2/DQS1B	CDPCLK2/DQS1B
B8	VREFB8N1	GND								
B8	VREFB8N1	IO	LVDS185n		AA5	AF5				
B8	VREFB8N1	GND								
B8	VREFB8N1	IO	LVDS184p			AD6			DQ1B3	
B8	VREFB8N1	IO	LVDS184n			AD7				
B8	VREFB8N1	VCCIO8								
B8	VREFB8N1	IO	VREFB8N1		Y7	AC7				
B8	VREFB8N1	GND								

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672
B8	VREFB8N1	IO				W8				
B8	VREFB8N1	IO	LVDS183p		U8	W10	DQ3B8	DQ3B17		
B8	VREFB8N1	IO	LVDS183n			Y10			DQ1B2	
B8	VREFB8N1	GND								
B8	VREFB8N1	IO				AB8			DQ1B1	
B8	VREFB8N1	IO	LVDS182p			AC8			DQ1B0	
B8	VREFB8N1	IO	LVDS182n			AD8			DM3B/BWS#3B	DM3B1/BWS#3B1
B8	VREFB8N1	IO	LVDS181p		AB6	AE6	DQ3B7	DQ3B16	DQ3B8	DQ3B17
B8	VREFB8N1	VCCIO8								
B8	VREFB8N1	IO	LVDS181n		AA6	AF6	DQ3B6	DQ3B15	DQ3B7	DQ3B16
B8	VREFB8N1	GND								
B8	VREFB8N1	IO				AA9			DQ3B6	DQ3B15
B8	VREFB8N1	IO	LVDS180p		V8	AA10	DQ3B5	DQ3B14	DQ3B5	DQ3B14
B8	VREFB8N1	IO	LVDS180n		W7	AB10	DQ3B4	DQ3B13	DQ3B4	DQ3B13
B8	VREFB8N1	GND								
B8	VREFB8N1	IO	LVDS179p		W8	AA11	DQ3B3	DQ3B12	DQ3B3	DQ3B12
B8	VREFB8N1	IO	LVDS179n		V9	Y11	DQ3B2	DQ3B11	DQ3B2	DQ3B11
B8	VREFB8N1	IO	LVDS178p		AB7	AE7	DQ3B1	DQ3B10	DQ3B1	DQ3B10
B8	VREFB8N1	IO	LVDS178n		AA7	AF7	DQ3B0	DQ3B9	DQ3B0	DQ3B9
B8	VREFB8N1	VCCIO8								
B8	VREFB8N0	IO	LVDS177p		Y9	AE8	DPCLK2/DQS3B	DPCLK2/DQS3B	DPCLK2/DQS3B	DPCLK2/DQS3B
B8	VREFB8N0	GND								
B8	VREFB8N0	IO	LVDS177n		W9	AF8				
B8	VREFB8N0	IO	LVDS176p			W11				
B8	VREFB8N0	IO	LVDS176n			W12				
B8	VREFB8N0	GND								
B8	VREFB8N0	IO	LVDS175p		U9	AC9	DM5B/BWS#5B	DM3B0/BWS#3B0	DM5B/BWS#5B	DM3B0/BWS#3B0
B8	VREFB8N0	IO	LVDS175n		U10	AC10	DQ5B8	DQ3B8		
B8	VREFB8N0	IO	LVDS174p			AE9			DQ5B8	DQ3B8
B8	VREFB8N0	VCCIO8								
B8	VREFB8N0	IO	LVDS174n			AF9			DQ5B7	DQ3B7
B8	VREFB8N0	GND								
B8	VREFB8N0	IO	LVDS173p			AD10			DQ5B6	DQ3B6
B8	VREFB8N0	IO	LVDS173n			AC11			DQ5B5	DQ3B5
B8	VREFB8N0	IO	LVDS172p		AB8	AE10	DQ5B7	DQ3B7	DQ5B4	DQ3B4
B8	VREFB8N0	GND								

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672
B8	VREFB8N0	IO	LVDS172n		AA8	AF10	DQ5B6	DQ3B6	DQ5B3	DQ3B3
B8	VREFB8N0	IO				AB12			DQ5B2	DQ3B2
B8	VREFB8N0	IO	VREFB8N0		Y10	AC12				
B8	VREFB8N0	IO	LVDS171p			AD11			DQ5B1	DQ3B1
B8	VREFB8N0	VCCIO8								
B8	VREFB8N0	IO	LVDS171n			AE11			DQ5B0	DQ3B0
B8	VREFB8N0	GND								
B8	VREFB8N0	IO	LVDS170p		AB9	V14	DQ5B5	DQ3B5		
B8	VREFB8N0	IO	LVDS170n		AA9	V13	DQ5B4	DQ3B4		
B8	VREFB8N0	GND								
B8	VREFB8N0	IO	LVDS169p		W11	AA12	DQ5B3	DQ3B3	DM4B	DM5B1/BWS#5B1
B8	VREFB8N0	IO	LVDS169n		V11	Y12	DQ5B2	DQ3B2		DQ5B17
B8	VREFB8N0	VCCIO8								
B8	VREFB8N0	IO	LVDS168p		AB10	AD12	DQ5B1	DQ3B1	DQ4B7	DQ5B16
B8	VREFB8N0	GND								
B8	VREFB8N0	IO	LVDS168n		AA10	AE12	DQ5B0	DQ3B0	DQ4B6	DQ5B15
B8	VREFB8N0	IO	LVDS167p		AB11	AE13	DPCLK3/DQS5B	DPCLK3/DQS5B	DPCLK3/DQS5B	DPCLK3/DQS5B
B8	VREFB8N0	GND								
B8	VREFB8N0	IO	LVDS167n		AA11	AF13				
B8	VREFB8N0	CLK15	LVDSCLK7p/input(3)		U11	AC13				
B8	VREFB8N0	CLK14	LVDSCLK7n/input(3)		U12	AD13				
B7	VREFB7N1	CLK13	LVDSCLK6p/input(3)		W12	AF14				
B7	VREFB7N1	CLK12	LVDSCLK6n/input(3)		V12	AE14				
B7	VREFB7N1	IO	LVDS166p		AB12	AE15	DPCLK4/DQS4B	DPCLK4/DQS4B	DPCLK4/DQS4B	DPCLK4/DQS4B
B7	VREFB7N1	VCCIO7								
B7	VREFB7N1	IO	LVDS166n		AA12	AD15				
B7	VREFB7N1	GND								
B7	VREFB7N1	IO				AC14			DQ4B5	DQ5B14
B7	VREFB7N1	GND								
B7	VREFB7N1	IO	LVDS165p			AA13			DQ4B4	DQ5B13
B7	VREFB7N1	IO	LVDS165n			Y13			DQ4B3	DQ5B12
B7	VREFB7N1	IO	LVDS164p		AB13	AA14	DM4B	DM5B1/BWS#5B1		
B7	VREFB7N1	IO	LVDS164n		AA13	Y14		DQ5B17	DQ4B2	DQ5B11
B7	VREFB7N1	IO	LVDS163p			Y15			DQ4B1	DQ5B10
B7	VREFB7N1	IO	LVDS163n			AA15			DQ4B0	DQ5B9
B7	VREFB7N1	VCCIO7								

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672
B7	VREFB7N1	IO	LVDS162p			AB15				
B7	VREFB7N1	GND								
B7	VREFB7N1	IO	LVDS162n		U13	AC15	DQ4B7	DQ5B16	DM2B	DM5B0/BWS#5B0
B7	VREFB7N1	GND								
B7	VREFB7N1	IO	LVDS161p			AE16				DQ5B8
B7	VREFB7N1	IO	LVDS161n			AD16			DQ2B7	DQ5B7
B7	VREFB7N1	IO	VREFB7N1		Y13	AC16				
B7	VREFB7N1	IO	LVDS160p		AB14	W15	DQ4B6	DQ5B15		
B7	VREFB7N1	VCCIO7								
B7	VREFB7N1	IO	LVDS160n		AA14	W16	DQ4B5	DQ5B14		
B7	VREFB7N1	GND								
B7	VREFB7N1	IO	LVDS159p		AB15	AF17	DQ4B4	DQ5B13	DQ2B6	DQ5B6
B7	VREFB7N1	GND								
B7	VREFB7N1	IO	LVDS159n		AA15	AE17	DQ4B3	DQ5B12	DQ2B5	DQ5B5
B7	VREFB7N1	IO	LVDS158p		AB16	AC17	DQ4B2	DQ5B11	DQ2B4	DQ5B4
B7	VREFB7N1	IO	LVDS158n		AA16	AD17	DQ4B1	DQ5B10	DQ2B3	DQ5B3
B7	VREFB7N1	IO	LVDS157p		W14	AA16	DQ4B0	DQ5B9	DQ2B2	DQ5B2
B7	VREFB7N1	IO	LVDS157n		V14	Y16	DM2B	DM5B0/BWS#5B0	DQ2B1	DQ5B1
B7	VREFB7N1	IO	LVDS156p			AF18			DQ2B0	DQ5B0
B7	VREFB7N1	VCCIO7								
B7	VREFB7N1	IO	LVDS156n			AE18				
B7	VREFB7N1	GND								
B7	VREFB7N1	IO	LVDS155p		AB17	AF19	DPCLK5/DQS2B	DPCLK5/DQS2B	DPCLK5/DQS2B	DPCLK5/DQS2B
B7	VREFB7N1	GND								
B7	VREFB7N1	IO	LVDS155n		AA17	AE19				
B7	VREFB7N0	IO	LVDS154p			AB18				
B7	VREFB7N0	IO	LVDS154n			AC18				
B7	VREFB7N0	IO	LVDS153p		U14	W17		DQ5B8		
B7	VREFB7N0	IO	LVDS153n			V17				
B7	VREFB7N0	VCCIO7								
B7	VREFB7N0	IO	LVDS152p		Y14	AA17	DQ2B7	DQ5B7		
B7	VREFB7N0	GND								
B7	VREFB7N0	IO	LVDS152n		W15	AA18	DQ2B6	DQ5B6		
B7	VREFB7N0	GND								
B7	VREFB7N0	IO	LVDS151p			AD19			DM0B	
B7	VREFB7N0	IO	LVDS151n			AC19				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672
B7	VREFB7N0	IO	LVDS150p			AF20			DQ0B7	
B7	VREFB7N0	IO	LVDS150n			AE20			DQ0B6	
B7	VREFB7N0	IO	LVDS149p			AB20			DQ0B5	
B7	VREFB7N0	IO	LVDS149n			AC20			DQ0B4	
B7	VREFB7N0	VCCIO7								
B7	VREFB7N0	IO	LVDS148p		AB18	AF21	DQ2B5	DQ5B5	DQ0B3	
B7	VREFB7N0	GND								
B7	VREFB7N0	IO	LVDS148n		AA18	AE21	DQ2B4	DQ5B4		
B7	VREFB7N0	GND								
B7	VREFB7N0	IO	VREFB7N0		Y16	Y18				
B7	VREFB7N0	IO				AA20			DQ0B2	
B7	VREFB7N0	VCCIO7								
B7	VREFB7N0	GND								
B7	VREFB7N0	IO	LVDS147p			AF22			DQ0B1	
B7	VREFB7N0	GND								
B7	VREFB7N0	IO	LVDS147n			AE22			DQ0B0	
B7	VREFB7N0	IO	LVDS146p		U15	AC21	CDPCLK3/DQS0B	CDPCLK3/DQS0B	CDPCLK3/DQS0B	CDPCLK3/DQS0B
B7	VREFB7N0	IO	LVDS146n		V15	AD21				
B7	VREFB7N0	VCCIO7								
B7	VREFB7N0	IO	LVDS145p		Y17	AD23	DQ2B3	DQ5B3		
B7	VREFB7N0	IO	LVDS145n		W16	AD22	DQ2B2	DQ5B2		
B7	VREFB7N0	IO	LVDS144p		AB19	AC22	DQ2B1	DQ5B1		
B7	VREFB7N0	IO	LVDS144n		AA19	AB21	DQ2B0	DQ5B0		
B7	VREFB7N0	IO	LVDS143p		AB20	AF23				
B7	VREFB7N0	IO	LVDS143n		AA20	AE23				
B7	VREFB7N0	GND								
B7	VREFB7N0	GNDA_PLL4			V16	Y19				
B7	VREFB7N0	VCCA_PLL4			U16	AA19				
B6	VREFB6N1	GND_PLL4			V18	AA21				
B6	VREFB6N1	VCCD_PLL4			U17	Y20				
B6	VREFB6N1	GND_PLL4			T17	W20				
B6	VREFB6N1	GND								
B6	VREFB6N1	IO			Y18	AC23				
B6	VREFB6N1	IO	LVDS142n	INIT_DONE	V19	AE25				
B6	VREFB6N1	IO	LVDS142p	nCEO	W20	AE24				
B6	VREFB6N1	IO	LVDS141n		Y19	AD25				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672
B6	VREFB6N1	IO	LVDS141p		Y20	AD24	DM3R/BWS#3R	DM3R1/BWS#3R1		
B6	VREFB6N1	IO				AC24				
B6	VREFB6N1	IO			W18	Y21				
B6	VREFB6N1	IO	PLL4_OUTn		U18	V20				
B6	VREFB6N1	VCCIO6								
B6	VREFB6N1	IO	PLL4_OUTp		T18	V21				
B6	VREFB6N1	IO	LVDS140n		U19	W21	DQ3R8	DQ3R17		
B6	VREFB6N1	IO	LVDS140p		V20	Y22	DQ3R7	DQ3R16		
B6	VREFB6N1	GND								
B6	VREFB6N1	IO	LVDS139n			AA24				
B6	VREFB6N1	IO	LVDS139p			AA23				
B6	VREFB6N1	IO	LVDS138n			AB24				
B6	VREFB6N1	IO	LVDS138p			AB23				
B6	VREFB6N1	IO	VREFB6N1		U20	V22				
B6	VREFB6N1	IO	LVDS137n		W21	AC25	DQ3R6	DQ3R15		
B6	VREFB6N1	IO	LVDS137p		W22	AC26	DQ3R5	DQ3R14		
B6	VREFB6N1	VCCIO6								
B6	VREFB6N1	IO	LVDS136n			AB26				
B6	VREFB6N1	IO	LVDS136p			AB25				
B6	VREFB6N1	IO	LVDS135n			Y24				
B6	VREFB6N1	IO	LVDS135p		R17	Y23	DQ3R4	DQ3R13		
B6	VREFB6N1	IO	LVDS134n			AA25				
B6	VREFB6N1	GND								
B6	VREFB6N1	IO	LVDS134p			AA26				
B6	VREFB6N1	GND								
B6	VREFB6N1	IO	LVDS133n		Y21	Y26	DQ3R3	DQ3R12	DM3R/BWS#3R	DM3R1/BWS#3R1
B6	VREFB6N1	IO	LVDS133p		Y22	Y25	DQ3R2	DQ3R11	DQ3R8	DQ3R17
B6	VREFB6N1	IO				U22			DQ3R7	DQ3R16
B6	VREFB6N1	IO	LVDS132n		V21	W24	DQ3R1	DQ3R10	DQ3R6	DQ3R15
B6	VREFB6N1	IO	LVDS132p		V22	W23	DQ3R0	DQ3R9	DQ3R5	DQ3R14
B6	VREFB6N1	IO	LVDS131n		U21	W25				
B6	VREFB6N1	VCCIO6								
B6	VREFB6N1	IO	LVDS131p		U22	W26	CDPCLK4/DQS3R	CDPCLK4/DQS3R	CDPCLK4/DQS3R	CDPCLK4/DQS3R
B6	VREFB6N0	IO	LVDS130n		R18	V23	DM1R/BWS#1R	DM3R0/BWS#3R0	DQ3R4	DQ3R13
B6	VREFB6N0	IO	LVDS130p		R19	V24	DQ1R8	DQ3R8	DQ3R3	DQ3R12
B6	VREFB6N0	IO	LVDS129n		P17	V25	DQ1R7	DQ3R7	DQ3R2	DQ3R11

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672
B6	VREFB6N0	IO	LVDS129p		P18	V26	DQ1R6	DQ3R6	DQ3R1	DQ3R10
B6	VREFB6N0	GND								
B6	VREFB6N0	IO	LVDS128n			U21			DQ3R0	DQ3R9
B6	VREFB6N0	IO	LVDS128p			U20				
B6	VREFB6N0	IO	LVDS127n		T21	T19	DQ1R5	DQ3R5		
B6	VREFB6N0	IO	LVDS127p		T22	R19	DQ1R4	DQ3R4		
B6	VREFB6N0	IO	LVDS126n		R21	U24	DQ1R3	DQ3R3		
B6	VREFB6N0	IO	LVDS126p		R22	U23	DQ1R2	DQ3R2	DM1R/BWS#1R	DM3R0/BWS#3R0
B6	VREFB6N0	IO	LVDS125n			U25			DQ1R8	DQ3R8
B6	VREFB6N0	VCCIO6								
B6	VREFB6N0	IO	LVDS125p			U26			DQ1R7	DQ3R7
B6	VREFB6N0	IO				T20			DQ1R6	DQ3R6
B6	VREFB6N0	IO	VREFB6N0		R20	T21				
B6	VREFB6N0	GND								
B6	VREFB6N0	IO	LVDS124n		P20	T25			DQ1R5	DQ3R5
B6	VREFB6N0	IO	LVDS124p		P19	T24			DQ1R4	DQ3R4
B6	VREFB6N0	VCCIO6								
B6	VREFB6N0	IO	LVDS123n		P21	T23				
B6	VREFB6N0	IO	LVDS123p		P22	T22			DQ1R3	DQ3R3
B6	VREFB6N0	IO				R20			DQ1R2	DQ3R2
B6	VREFB6N0	nSTATUS		nSTATUS	N20	R22				
B6	VREFB6N0	GND								
B6	VREFB6N0	CONF_DONE		CONF_DONE	N18	R23				
B6	VREFB6N0	GND								
B6	VREFB6N0	MSEL1		MSEL1	N17	P21				
B6	VREFB6N0	MSEL0		MSEL0	M17	P20				
B6	VREFB6N0	IO	LVDS122n		N21	R24	DQ1R1	DQ3R1	DQ1R1	DQ3R1
B6	VREFB6N0	IO	LVDS122p		N22	R25	DQ1R0	DQ3R0	DQ1R0	DQ3R0
B6	VREFB6N0	VCCIO6								
B6	VREFB6N0	IO	LVDS121n		M19	P24				
B6	VREFB6N0	IO	LVDS121p		M18	P23	DPCLK6/DQS1R	DPCLK6/DQS1R	DPCLK6/DQS1R	DPCLK6/DQS1R
B6	VREFB6N0	CLK7	LVDSCLK3n/input(3)		M21	P26				
B6	VREFB6N0	CLK6	LVDSCLK3p/input(3)		M22	P25				
B5	VREFB5N1	CLK5	LVDSCLK2n/input(3)		L21	N26				
B5	VREFB5N1	CLK4	LVDSCLK2p/input(3)		L22	N25				
B5	VREFB5N1	IO	LVDS120n		L19	N24				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672
B5	VREFB5N1	IO	LVDS120p		L18	N23	DPCLK7/DQS0R	DPCLK7/DQS0R	DPCLK7/DQS0R	DPCLK7/DQS0R
B5	VREFB5N1	IO				N21				
B5	VREFB5N1	IO	LVDS119n		K21	M25	DM0R	DM1R1/BWS#1R1	DM0R	DM1R1/BWS#1R1
B5	VREFB5N1	GND								
B5	VREFB5N1	IO	LVDS119p		K22	M24		DQ1R17		DQ1R17
B5	VREFB5N1	VCCIO5								
B5	VREFB5N1	IO	LVDS118n		J21	M21	DQ0R7	DQ1R16		
B5	VREFB5N1	IO	LVDS118p		J22	N20	DQ0R6	DQ1R15	DQ0R7	DQ1R16
B5	VREFB5N1	GND								
B5	VREFB5N1	IO	LVDS117n		L17	M20			DQ0R6	DQ1R15
B5	VREFB5N1	IO	LVDS117p		K17	M19			DQ0R5	DQ1R14
B5	VREFB5N1	IO	LVDS116n		H21	M23			DQ0R4	DQ1R13
B5	VREFB5N1	IO	LVDS116p		H22	M22			DQ0R3	DQ1R12
B5	VREFB5N1	IO	LVDS115n			K26			DQ0R2	DQ1R11
B5	VREFB5N1	VCCIO5								
B5	VREFB5N1	IO	LVDS115p			K25			DQ0R1	DQ1R10
B5	VREFB5N1	IO			K18	L19			DQ0R0	DQ1R9
B5	VREFB5N1	IO	LVDS114n		J20	L25	DQ0R5	DQ1R14		
B5	VREFB5N1	IO	LVDS114p		H19	L24	DQ0R4	DQ1R13		
B5	VREFB5N1	IO	VREFB5N1		K20	L23				
B5	VREFB5N1	GND								
B5	VREFB5N1	IO	LVDS113n			J26				
B5	VREFB5N1	GND								
B5	VREFB5N1	IO	LVDS113p			J25				
B5	VREFB5N1	IO	LVDS112n			L20				
B5	VREFB5N1	IO	LVDS112p			L21				
B5	VREFB5N1	IO	LVDS111n		J19	K24	DQ0R3	DQ1R12	DM2R	DM1R0/BWS#1R0
B5	VREFB5N1	IO	LVDS111p		J18	K23	DQ0R2	DQ1R11		DQ1R8
B5	VREFB5N1	IO				K21			DQ2R7	DQ1R7
B5	VREFB5N1	VCCIO5								
B5	VREFB5N1	IO			J17	K19	DQ0R1	DQ1R10	DQ2R6	DQ1R6
B5	VREFB5N1	IO	LVDS110n			H26			DQ2R5	DQ1R5
B5	VREFB5N1	GND								
B5	VREFB5N1	IO	LVDS110p			H25			DQ2R4	DQ1R4
B5	VREFB5N1	GND								
B5	VREFB5N1	IO	LVDS109n		G21	J24	DQ0R0	DQ1R9	DQ2R3	DQ1R3

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672
B5	VREFB5N1	IO	LVDS109p		G22	J23	DM2R	DM1R0/BWS#1R0	DQ2R2	DQ1R2
B5	VREFB5N1	IO	LVDS108n			H24			DQ2R1	DQ1R1
B5	VREFB5N1	IO	LVDS108p			H23			DQ2R0	DQ1R0
B5	VREFB5N0	IO	LVDS107n		F21	G26				
B5	VREFB5N0	IO	LVDS107p		F22	G25	CDPCLK5/DQS2R	CDPCLK5/DQS2R	CDPCLK5/DQS2R	CDPCLK5/DQS2R
B5	VREFB5N0	IO				K22				
B5	VREFB5N0	VCCIO5								
B5	VREFB5N0	IO	LVDS106n		H18	G24		DQ1R8		
B5	VREFB5N0	IO	LVDS106p		H17	G23	DQ2R7	DQ1R7		
B5	VREFB5N0	IO	LVDS105n			P18				
B5	VREFB5N0	IO	LVDS105p			N18				
B5	VREFB5N0	IO	LVDS104n		E21	F26	DQ2R6	DQ1R6		
B5	VREFB5N0	GND								
B5	VREFB5N0	IO	LVDS104p		E22	F25	DQ2R5	DQ1R5		
B5	VREFB5N0	IO	LVDS103n		D21	J20	DQ2R4	DQ1R4		
B5	VREFB5N0	IO	LVDS103p		D22	J21				
B5	VREFB5N0	IO	LVDS102n		G17	F23	DQ2R3	DQ1R3		
B5	VREFB5N0	IO	LVDS102p		G18	F24	DQ2R2	DQ1R2		
B5	VREFB5N0	IO	LVDS101n			E25				
B5	VREFB5N0	IO	LVDS101p			E26				
B5	VREFB5N0	VCCIO5								
B5	VREFB5N0	IO	VREFB5N0		G20	J22				
B5	VREFB5N0	IO	LVDS100n		E20	D25	DQ2R1	DQ1R1		
B5	VREFB5N0	IO	LVDS100p		F20	D26	DQ2R0	DQ1R0		
B5	VREFB5N0	IO	LVDS99n		C21	C24				
B5	VREFB5N0	IO	LVDS99p		C22	C25				
B5	VREFB5N0	GND								
B5	VREFB5N0	IO	LVDS98n			B25				
B5	VREFB5N0	IO	LVDS98p			B24				
B5	VREFB5N0	IO	LVDS97n			E24				
B5	VREFB5N0	IO	LVDS97p			E23				
B5	VREFB5N0	IO				H21				
B5	VREFB5N0	VCCIO5								
B5	VREFB5N0	IO	LVDS96n		C19	G22				
B5	VREFB5N0	IO	LVDS96p		C20	G21				
B5	VREFB5N0	IO	LVDS95n		D19	D23				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672
B5	VREFB5N0	IO	LVDS95p		D20	E22				
B5	VREFB5N0	IO	PLL2_OUTp		E19	F21				
B5	VREFB5N0	IO	PLL2_OUTn		E18	F20				
B5	VREFB5N0	GND								
B5	VREFB5N0	GND_PLL2			F18	G20				
B5	VREFB5N0	VCCD_PLL2			F17	H20				
B5	VREFB5N0	GND_PLL2			E17	E21				
B4	VREFB4N0	VCCA_PLL2			F16	G19				
B4	VREFB4N0	GNDA_PLL2			E16	F19				
B4	VREFB4N0	GND								
B4	VREFB4N0	IO	LVDS94n		C18	C23				
B4	VREFB4N0	IO	LVDS94p		C17	C22				
B4	VREFB4N0	IO	LVDS93n		B20	C21	DQ2T0	DQ5T0		
B4	VREFB4N0	IO	LVDS93p		A20	D21	DQ2T1	DQ5T1		
B4	VREFB4N0	IO	LVDS92n		B19	B23	DQ2T2	DQ5T2		
B4	VREFB4N0	IO	LVDS92p		A19	A23	DQ2T3	DQ5T3		
B4	VREFB4N0	VCCIO4								
B4	VREFB4N0	IO	LVDS91n		B18	A22				
B4	VREFB4N0	IO	LVDS91p		A18	B22	CDPCLK6/DQS0T	CDPCLK6/DQS0T	CDPCLK6/DQS0T	CDPCLK6/DQS0T
B4	VREFB4N0	IO	LVDS90n			B21			DQ0T0	
B4	VREFB4N0	GND								
B4	VREFB4N0	IO	LVDS90p			A21			DQ0T1	
B4	VREFB4N0	GND								
B4	VREFB4N0	VCCIO4								
B4	VREFB4N0	IO				D20			DQ0T2	
B4	VREFB4N0	IO	VREFB4N0		C16	E20				
B4	VREFB4N0	GND								
B4	VREFB4N0	IO	LVDS89n		D16	B20	DQ2T4	DQ5T4		
B4	VREFB4N0	GND								
B4	VREFB4N0	IO	LVDS89p		E15	A20	DQ2T5	DQ5T5	DQ0T3	
B4	VREFB4N0	VCCIO4								
B4	VREFB4N0	IO	LVDS88n			C19			DQ0T4	
B4	VREFB4N0	IO	LVDS88p			D19			DQ0T5	
B4	VREFB4N0	IO	LVDS87n			B19			DQ0T6	
B4	VREFB4N0	IO	LVDS87p			A19			DQ0T7	
B4	VREFB4N0	IO	LVDS86n			E18				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672
B4	VREFB4N0	IO	LVDS86p			D18			DM0T	
B4	VREFB4N0	GND								
B4	VREFB4N0	IO	LVDS85n		D15	G18	DQ2T6	DQ5T6		
B4	VREFB4N0	GND								
B4	VREFB4N0	IO	LVDS85p		C14	F18	DQ2T7	DQ5T7		
B4	VREFB4N0	VCCIO4								
B4	VREFB4N0	IO	LVDS84n			J17				
B4	VREFB4N0	IO	LVDS84p		F15	H17		DQ5T8		
B4	VREFB4N0	IO	LVDS83n			F17				
B4	VREFB4N0	IO	LVDS83p			G17				
B4	VREFB4N1	IO	LVDS82n		B17	D17				
B4	VREFB4N1	GND								
B4	VREFB4N1	IO	LVDS82p		A17	C17	DPCLK8/DQS2T	DPCLK8/DQS2T	DPCLK8/DQS2T	DPCLK8/DQS2T
B4	VREFB4N1	GND								
B4	VREFB4N1	IO	LVDS81n			B18				
B4	VREFB4N1	VCCIO4								
B4	VREFB4N1	IO	LVDS81p			A18			DQ2T0	DQ5T0
B4	VREFB4N1	IO	LVDS80n		E14	G16	DM2T	DM5T0/BWS#5T0	DQ2T1	DQ5T1
B4	VREFB4N1	IO	LVDS80p		D14	F16	DQ4T0	DQ5T9	DQ2T2	DQ5T2
B4	VREFB4N1	IO	LVDS79n		F14	F15	DQ4T1	DQ5T10	DQ2T3	DQ5T3
B4	VREFB4N1	IO	LVDS79p		F13	G15	DQ4T2	DQ5T11	DQ2T4	DQ5T4
B4	VREFB4N1	IO	LVDS78n		B16	B17	DQ4T3	DQ5T12	DQ2T5	DQ5T5
B4	VREFB4N1	GND								
B4	VREFB4N1	IO	LVDS78p		A16	A17	DQ4T4	DQ5T13	DQ2T6	DQ5T6
B4	VREFB4N1	GND								
B4	VREFB4N1	IO	LVDS77n		B15	H16	DQ4T5	DQ5T14		
B4	VREFB4N1	VCCIO4								
B4	VREFB4N1	IO	LVDS77p		A15	H15	DQ4T6	DQ5T15		
B4	VREFB4N1	IO	VREFB4N1		C13	D16				
B4	VREFB4N1	IO	LVDS76n			E15			DQ2T7	DQ5T7
B4	VREFB4N1	IO	LVDS76p			D15				DQ5T8
B4	VREFB4N1	GND								
B4	VREFB4N1	IO	LVDS75n		F12	C16	DQ4T7	DQ5T16	DM2T	DM5T0/BWS#5T0
B4	VREFB4N1	GND								
B4	VREFB4N1	IO	LVDS75p			B16			DQ4T0	DQ5T9
B4	VREFB4N1	VCCIO4								

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672
B4	VREFB4N1	IO	LVDS74n			B15			DQ4T1	DQ5T10
B4	VREFB4N1	IO	LVDS74p			C15			DQ4T2	DQ5T11
B4	VREFB4N1	IO	LVDS73n		B14	G13		DQ5T17	DQ4T3	DQ5T12
B4	VREFB4N1	IO	LVDS73p		A14	F13	DM4T	DM5T1/BWS#5T1		
B4	VREFB4N1	IO	LVDS72n			G14			DQ4T4	DQ5T13
B4	VREFB4N1	IO	LVDS72p			F14			DQ4T5	DQ5T14
B4	VREFB4N1	GND								
B4	VREFB4N1	IO				D14			DQ4T6	DQ5T15
B4	VREFB4N1	GND								
B4	VREFB4N1	IO	LVDS71n		B13	A14				
B4	VREFB4N1	VCCIO4								
B4	VREFB4N1	IO	LVDS71p		A13	B14	DPCLK9/DQS4T	DPCLK9/DQS4T	DPCLK9/DQS4T	DPCLK9/DQS4T
B4	VREFB4N1	CLK8	LVDSCLK4n/input(3)		B12	B13				
B4	VREFB4N1	CLK9	LVDSCLK4p/input(3)		A12	A13				
B3	VREFB3N0	CLK10	LVDSCLK5n/input(3)		D12	C13				
B3	VREFB3N0	CLK11	LVDSCLK5p/input(3)		E12	D13				
B3	VREFB3N0	IO	LVDS70n		B11	B12				
B3	VREFB3N0	GND								
B3	VREFB3N0	IO	LVDS70p		A11	C12	DPCLK10/DQS5T	DPCLK10/DQS5T	DPCLK10/DQS5T	DPCLK10/DQS5T
B3	VREFB3N0	IO	LVDS69n		E11	B11	DQ5T0	DQ3T0	DQ4T7	DQ5T16
B3	VREFB3N0	GND								
B3	VREFB3N0	IO	LVDS69p		D11	C11	DQ5T1	DQ3T1		DQ5T17
B3	VREFB3N0	VCCIO3								
B3	VREFB3N0	IO	LVDS68n		B10	G12	DQ5T2	DQ3T2	DM4T	DM5T1/BWS#5T1
B3	VREFB3N0	IO	LVDS68p		A10	F12	DQ5T3	DQ3T3	DQ5T0	DQ3T0
B3	VREFB3N0	GND								
B3	VREFB3N0	IO	LVDS67n		F11	J14	DQ5T4	DQ3T4		
B3	VREFB3N0	IO	LVDS67p		F10	J13	DQ5T5	DQ3T5		
B3	VREFB3N0	GND								
B3	VREFB3N0	IO	LVDS66n			D12			DQ5T1	DQ3T1
B3	VREFB3N0	VCCIO3								
B3	VREFB3N0	IO	LVDS66p			E12			DQ5T2	DQ3T2
B3	VREFB3N0	IO	VREFB3N0		C10	D11				
B3	VREFB3N0	IO				G11			DQ5T3	DQ3T3
B3	VREFB3N0	IO	LVDS65n		B9	A10	DQ5T6	DQ3T6	DQ5T4	DQ3T4
B3	VREFB3N0	GND								

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672
B3	VREFB3N0	IO	LVDS65p		A9	B10	DQ5T7	DQ3T7	DQ5T5	DQ3T5
B3	VREFB3N0	IO	LVDS64n			D10			DQ5T6	DQ3T6
B3	VREFB3N0	IO	LVDS64p			C10			DQ5T7	DQ3T7
B3	VREFB3N0	GND								
B3	VREFB3N0	IO	LVDS63n			A9			DQ5T8	DQ3T8
B3	VREFB3N0	VCCIO3								
B3	VREFB3N0	IO	LVDS63p			B9			DM5T/BWS#5T	DM3T0/BWS#3T0
B3	VREFB3N0	IO	LVDS62n		E9	E10	DQ5T8	DQ3T8		
B3	VREFB3N0	IO	LVDS62p		D9	F11	DM5T/BWS#5T	DM3T0/BWS#3T0	DQ3T0	DQ3T9
B3	VREFB3N0	GND								
B3	VREFB3N0	IO	LVDS61n			H12				
B3	VREFB3N0	IO	LVDS61p			H11				
B3	VREFB3N0	IO	LVDS60n		B8	A8				
B3	VREFB3N0	GND								
B3	VREFB3N0	IO	LVDS60p		A8	B8	DPCLK11/DQS3T	DPCLK11/DQS3T	DPCLK11/DQS3T	DPCLK11/DQS3T
B3	VREFB3N1	VCCIO3								
B3	VREFB3N1	IO	LVDS59n		B7	C9	DQ3T0	DQ3T9	DQ3T1	DQ3T10
B3	VREFB3N1	IO	LVDS59p		A7	D9	DQ3T1	DQ3T10	DQ3T2	DQ3T11
B3	VREFB3N1	IO	LVDS58n		F9	G10	DQ3T2	DQ3T11	DQ3T3	DQ3T12
B3	VREFB3N1	IO	LVDS58p		E8	F10	DQ3T3	DQ3T12	DQ3T4	DQ3T13
B3	VREFB3N1	GND								
B3	VREFB3N1	IO	LVDS57n		D8	C8	DQ3T4	DQ3T13	DQ3T5	DQ3T14
B3	VREFB3N1	IO	LVDS57p		C9	D8	DQ3T5	DQ3T14	DQ3T6	DQ3T15
B3	VREFB3N1	IO	LVDS56n			A7			DQ3T7	DQ3T16
B3	VREFB3N1	GND								
B3	VREFB3N1	IO	LVDS56p		D7	B7	DQ3T6	DQ3T15	DQ3T8	DQ3T17
B3	VREFB3N1	VCCIO3								
B3	VREFB3N1	IO			F8	D6	DQ3T7	DQ3T16	DM3T/BWS#3T	DM3T1/BWS#3T1
B3	VREFB3N1	IO	LVDS55n			C7			DQ1T0	
B3	VREFB3N1	IO	LVDS55p			D7			DQ1T1	
B3	VREFB3N1	IO				F9			DQ1T2	
B3	VREFB3N1	GND								
B3	VREFB3N1	IO	LVDS54n			G9			DQ1T3	
B3	VREFB3N1	IO	LVDS54p		E7	H10	DQ3T8	DQ3T17		
B3	VREFB3N1	IO				H8				
B3	VREFB3N1	GND								

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672
B3	VREFB3N1	IO	VREFB3N1		C7	E8				
B3	VREFB3N1	VCCIO3								
B3	VREFB3N1	IO	LVDS53n			D5				
B3	VREFB3N1	IO	LVDS53p			C4			DQ1T4	
B3	VREFB3N1	GND								
B3	VREFB3N1	IO	LVDS52n		B6	A6				
B3	VREFB3N1	GND								
B3	VREFB3N1	IO	LVDS52p		A6	B6	CDPCLK7/DQS1T	CDPCLK7/DQS1T	CDPCLK7/DQS1T	CDPCLK7/DQS1T
B3	VREFB3N1	VCCIO3								
B3	VREFB3N1	IO	LVDS51n		B5	B5	DM3T/BWS#3T	DM3T1/BWS#3T1	DQ1T5	
B3	VREFB3N1	IO	LVDS51p		A5	A5			DQ1T6	
B3	VREFB3N1	IO	LVDS50n		B4	B4			DQ1T7	
B3	VREFB3N1	IO	LVDS50p		A4	A4			DM1T	
B3	VREFB3N1	IO	LVDS49p		A3	C6				
B3	VREFB3N1	IO	LVDS49n	DEV_CLRn	B3	C5				
B3	VREFB3N1	GND								
B3	VREFB3N1	GNDA_PLL3			F7	F8				
B3	VREFB3N1	VCCA_PLL3			E6	G8				
		VCCINT			G7	H19				
		VCCINT			G8	J9				
		VCCINT			G12	J18				
		VCCINT			G16	K9				
		VCCINT			H7	K10				
		VCCINT			H8	K11				
		VCCINT			H12	K12				
		VCCINT			H13	K13				
		VCCINT			H16	K14				
		VCCINT			J10	K15				
		VCCINT			J11	K18				
		VCCINT			J12	L9				
		VCCINT			J13	L11				
		VCCINT			K8	L16				
		VCCINT			K9	L17				
		VCCINT			K14	L18				
		VCCINT			L7	M10				
		VCCINT			L8	M11				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672
		VCCINT			L9	M16				
		VCCINT			L14	M17				
		VCCINT			L16	N10				
		VCCINT			M9	N17				
		VCCINT			M14	P10				
		VCCINT			M15	P17				
		VCCINT			N9	R10				
		VCCINT			N14	R11				
		VCCINT			N15	R16				
		VCCINT			P10	T9				
		VCCINT			P11	T11				
		VCCINT			P12	T16				
		VCCINT			P13	T18				
		VCCINT			P14	U9				
		VCCINT			R7	U11				
		VCCINT			R8	U13				
		VCCINT			R10	U14				
		VCCINT			R12	U15				
		VCCINT			R15	U16				
		VCCINT			R16	U18				
		VCCINT			T7	V9				
		VCCINT			T8	V10				
		VCCINT			T12	V16				
		VCCINT			T15	V18				
		VCCIO2			B1	C1				
		VCCIO2				F5				
		VCCIO2			J7	L1				
		VCCIO2				M9				
		VCCIO2			L3					
		VCCIO2				N5				
		VCCIO1			AA1	AB5				
		VCCIO1			M3	AD1				
		VCCIO1				P5				
		VCCIO1			P7	R9				
		VCCIO1				T1				
		VCCIO1			T4	V8				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672
		VCCIO8			AB2	AB6				
		VCCIO8				AB9				
		VCCIO8			T9	AB13				
		VCCIO8			V10	AF3				
		VCCIO8				AF11				
		VCCIO8			W6	V12				
		VCCIO8			Y11	W9				
		VCCIO7			AB21	AB14				
		VCCIO7				AB17				
		VCCIO7			T14	AB22				
		VCCIO7			V13	AD20				
		VCCIO7				AF16				
		VCCIO7			W17	AF24				
		VCCIO7				V15				
		VCCIO7			Y12	W18				
		VCCIO6			AA22	AA22				
		VCCIO6				AD26				
		VCCIO6			M20	P22				
		VCCIO6				R18				
		VCCIO6			P16	T26				
		VCCIO6			T19	V19				
		VCCIO5			B22	C26				
		VCCIO5				F22				
		VCCIO5			G19	J19				
		VCCIO5			J16	L26				
		VCCIO5				M18				
		VCCIO5			L20	N22				
		VCCIO4			A21	A16				
		VCCIO4				A24				
		VCCIO4			C12	C20				
		VCCIO4				D22				
		VCCIO4			D17	E14				
		VCCIO4			E13	E17				
		VCCIO4				H18				
		VCCIO4			G14	J15				
		VCCIO3			A2	A3				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672
		VCCIO3			C6	A11				
		VCCIO3				E6				
		VCCIO3			C11	E9				
		VCCIO3			E10	E13				
		VCCIO3				H9				
		VCCIO3			G9	J12				
		GND			G11	J10				
		GND			G15	J11				
		GND			H9	J16				
		GND			H10	K16				
		GND			H11	K17				
		GND			H14	L10				
		GND			H15	L12				
		GND			J8	L13				
		GND			J9	L14				
		GND			J14	L15				
		GND			J15	M12				
		GND			K10	M13				
		GND			K11	M14				
		GND			K12	M15				
		GND			K13	N11				
		GND			K15	N12				
		GND			L10	N13				
		GND			L11	N14				
		GND			L12	N15				
		GND			L13	N16				
		GND			L15	P11				
		GND			M7	P12				
		GND			M8	P13				
		GND			M10	P14				
		GND			M11	P15				
		GND			M12	P16				
		GND			M13	R12				
		GND			M16	R13				
		GND			N8	R14				
		GND			N10	R15				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672
		GND			N11	R17				
		GND			N12	T10				
		GND			N13	T12				
		GND			P8	T13				
		GND			P9	T14				
		GND			P15	T15				
		GND			R9	T17				
		GND			R11	U10				
		GND			R13	U12				
		GND			R14	U17				
		GND			T11	V11				
		GND			T16	W19				
		GND			A1	A2				
		GND				A12				
		GND			A22	A15				
		GND				A25				
		GND			AA2					
		GND				AB7				
		GND			AA21	AB11				
		GND			AB1	AB16				
		GND				AB19				
		GND			AB22	AC4				
		GND				AD9				
		GND			B2	AD14				
		GND			B21	AD18				
		GND			C5					
		GND				AE1				
		GND			C8	AE26				
		GND			C15	AF2				
		GND				AF12				
		GND			D10	AF15				
		GND			D13	AF25				
		GND			D18	B1				
		GND				B26				
		GND			F19	C14				
		GND			G4	C18				

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672
		GND				D4				
		GND			G10	D24				
		GND			G13	E7				
		GND			H20	E11				
		GND			K3	E16				
		GND			K7	E19				
		GND				H5				
		GND			K16	H13				
		GND				H14				
		GND			K19	H22				
		GND			M4	K20				
		GND				L5				
		GND			N7	L22				
		GND			N16	M1				
		GND				M26				
		GND			N19	N8				
		GND			R3	N19				
		GND			T10	P8				
		GND			T13	P19				
		GND				R1				
		GND			T20	R21				
		GND			V3	R26				
		GND				T5				
		GND			V6	U8				
		GND			V17	U19				
		GND			W10	W5				
		GND				W13				
		GND			W13	W14				
		GND			W19	W22				
		GND				Y9				
		GND			Y8					
		GND			Y15	Y17				

Notes:
(1) Optional Functions (LVDS, DDR, etc) are not available for some pins in certain packages. E.g. for EP2C8, LVDS70 pair is available for Q208 and F256 but not for T144.
(2) DQS0T, DQS1T, DQS0B and DQS1B pin functions are only available in F672 and F896 packages.

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	F484/ U484	F672	DQS for x8/x9 in F484/U484	DQS for x16/x18 in F484/U484	DQS for x8/x9 in F672	DQS for x16/x18 in F672

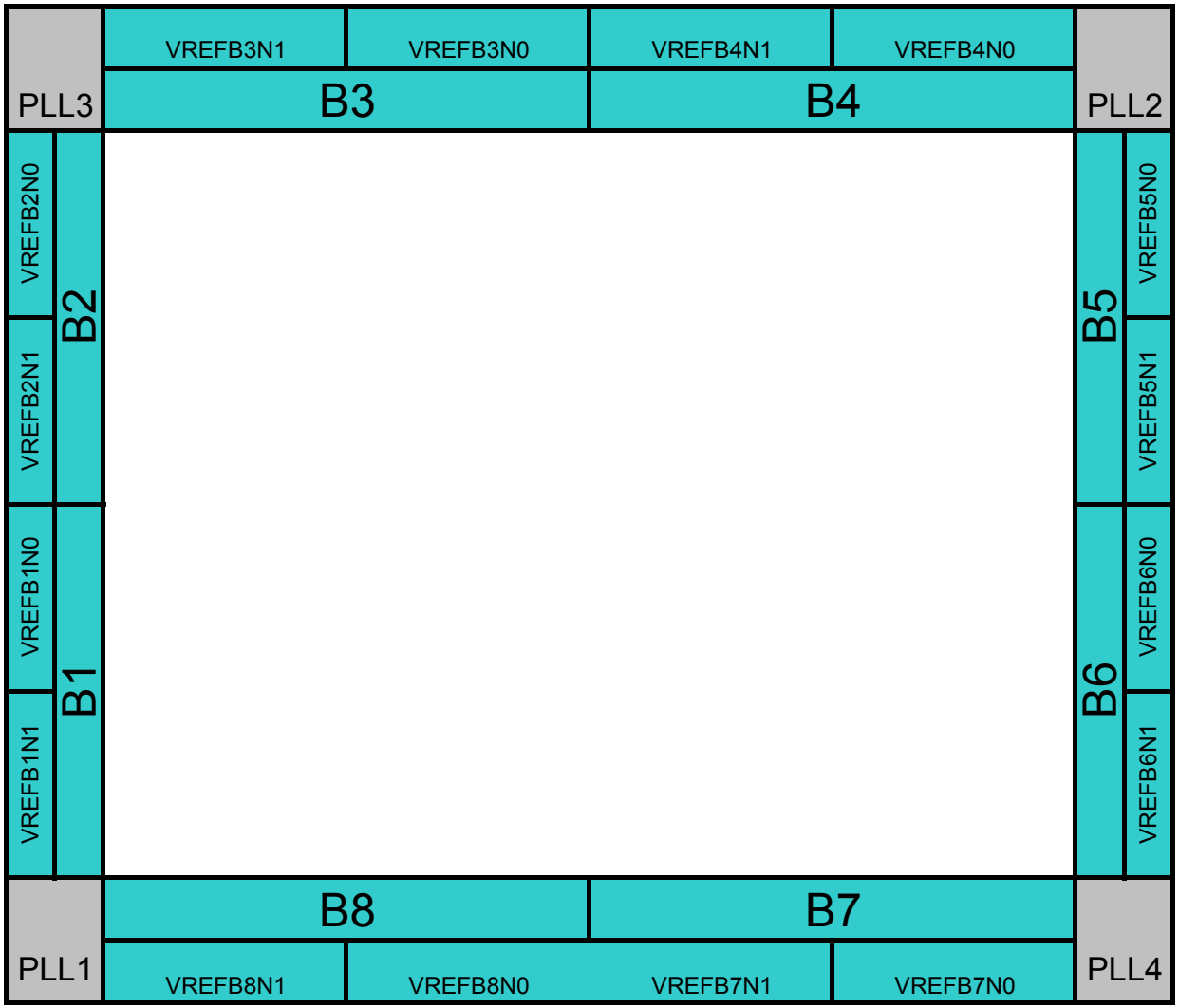
(3) If the dedicated CLK pins are not used to feed the global clock networks, they can be used as general-purpose input pins to feed core logic. They do not have support for an I/O register.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
	Supply and Reference Pins	
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVPECL, LVDS(regular I/O and CLK pins) ,differential HSTL and differential SSTL I/O standards. All VCCINT pins must be connected to 1.2 V.
VCCIO[1..8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5 V, 1.8 V, 2.5 V, 3.3-V PCI, and 3.3-V PCI-X,differential SSTL, differential HSTL, and LVDS (regular I/O) I/O standards.
GND	Ground	Device ground pins. All GND pins should be connected to the board GND plane.
VREFB[1..8]N[0..1]	I/O	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins.
VCCA_PLL[1..4]	Power	Analog power for PLLs[1..4]. The designer must connect these pins to 1.2 V, even if the PLL is not used. Designer is advised to keep isolated from other VCC for better jitter performance.
VCCD_PLL[1..4]	Power	Digital power for PLLs[1..4]. The designer must connect these pins to 1.2 V, even if the PLL is not used.
GNDA_PLL[1..4]	Ground	Analog ground for PLLs[1..4]. The designer can connect this pin to the GND plane on the board.
GND_PLL[1..4]	Ground	Ground for PLLs[1..4]. The designer can connect this pin to the GND plane on the board.
NC	No Connect	Do not drive signals into these pins.
	Dedicated Configuration/JTAG Pins	
DCLK	Input (PS) Output (AS)	Dedicated configuration clock pin. In PS configuration, DCLK is used to clock configuration data from an external source into the Cyclone II device. In AS mode, DCLK is an output from the Cyclone II device that provides timing for the configuration interface. DCLK should not be left floating. Designer should drive it high or low, whichever is more convenient on the board. The input buffer on this pin supports hysteresis using Schmitt or (Schmidt) trigger circuitry.
DATA0	Input	Dedicated configuration data input pin. In serial configuration modes, bit-wide configuration data is received through this pin. In AS mode, DATA0 has an internal pull-up resistor that is always active. The input buffer on this pin supports hysteresis using Schmitt or (Schmidt) trigger circuitry.
MSEL[0..1]	Input	Configuration input pins that set the Cyclone II device configuration scheme. These pins must be hard-wired to VCCPD or GND. The designer should connect MSEL[0..1] to 00 for AS, 10 for PS, 01 for Fast AS and 00 for JTAG-based Configuration.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled. In multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In single device configuration, nCE is tied low. The input buffer on this pin supports hysteresis using Schmitt or (Schmidt) trigger circuitry.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state & tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration. If the configuration scheme uses an enhanced configuration device or EPC2, nCONFIG can be tied directly to the configuration device's nINIT_CONF pin. If JTAG configuration is used, nCONFIG can be tied to VCC. The input buffer on this pin supports hysteresis using Schmitt or (Schmidt) trigger circuitry.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin. CONF_DONE should be pulled high by an external 10-kΩ pull-up resistor. The input buffer on this pin supports hysteresis using Schmitt or (Schmidt) trigger circuitry.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin. nSTATUS should be pulled high by an external 10-kΩ pull-up resistor. The input buffer on this pin supports hysteresis using Schmitt or (Schmidt) trigger circuitry.
TCK	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TCK to GND. The input buffer on this pin supports hysteresis using Schmitt or (Schmidt) trigger circuitry.
TMS	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TMS to VCC. The input buffer on this pin supports hysteresis using Schmitt or (Schmidt) trigger circuitry.
TDI	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TDI to VCC. The input buffer on this pin supports hysteresis using Schmitt or (Schmidt) trigger circuitry.
TDO	Output	Dedicated JTAG output pin. The JTAG circuitry can be disabled by leaving TDO unconnected.
Clock and PLL Pins		
CLK[0,2,4,6,9,11,13,15], LVDSCLK[0..7]p	Clock, Input	Dedicated global clock input pins that can also be used for the positive terminal inputs for differential global clock input or user input pins.
CLK[1,3,5,7,8,10,12,14], LVDSCLK[0..7]n	Clock, Input	Dedicated global clock input pins that can also be used for the negative terminal inputs for differential global clock input or user input pins.
PLL[1..4]_OUTp	I/O, Output	Optional positive terminal for external clock outputs from PLL [1..4]. These pins can only use the differential I/O standard if it is being fed by a PLL output

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
PLL[1..4]_OUTn	I/O, Output	Optional negative terminal for external clock outputs from PLL[1..4]. These pins can only use the differential I/O standard if it is being fed by a PLL output
Optional/Dual-Purpose Configuration Pins		
nCEO	I/O, Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin and must be pulled high to Vccio by an external 10kΩ pull-up resistor. During single device configuration and for the last device in multi-device configuration, this pin can be used as an user I/O after configuration.
nCSO	I/O, Output	Output control signal from the Cyclone II FPGA to the nCS pin of the serial configuration device in AS mode that enables the configuration device by driving it low. In AS mode, the nCSO has internal weak pull-up resistor, which is always active.
ASDO	I/O, Output	Output control signal from the Cyclone II FPGA to the serial configuration device in AS mode used to read out configuration data. In AS mode, the ASDO has internal weak pull-up resistor, which is always active.
CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.
DEV_CLRn	I/O (when option off), Input (when option on)	Optional chip-wide reset pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. The DEV_CLRn pin does not affect JTAG boundary-scan or programming operations. This pin is enabled by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus II software.
DEV_OE	I/O (when option off), Input (when option on)	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose status pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software.
Dual-Purpose Differential & External Memory Interface Pins		

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
LVDS[0-188][p,n]	I/O, TX/RX channel	Dual-purpose differential transmitter/receiver channels 0 to 188. These channels can be used for transmitting/receiving LVDS compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DPCLK[0..11]/ DQS[[0,1]L,[3,5,4,2]B,[1,0]R,[2,4,5,3]T]	I/O, DPCLK/DQS	Dual-purpose DPCLK/DQS pins can connect to the global clock network for high-fanout control signals such as clocks, asynchronous clears, presets and clock enables. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry, which allows fine tune of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.
CDPCLK[0..7]/ DQS[[2,3]L,[1,0]B,[3,2]R,[0,1]T]	I/O, CDPCLK/DQS	Dual-purpose CDPCLK/DQS pins can connect to the global clock network for high-fanout control signals such as clocks, asynchronous clears, presets and clock enables. Only one of the two CDPCLK in each corner can feed the clock control block at a time. The other pin can be used as general-purpose I/O pin. The CDPCLK signals incur more delay to the clock block control because they are multiplexed before driving into the clock block control. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry, which allows fine tune of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.
DQ[[[1,3][L,R]],[[3,5][B,T]]][0..17]	I/O, DQ	Optional data signal for use in external memory interfacing in the x16 or x18 modes.
DQ[[[0..3][L,R]],[[0..5][B,T]]][0..8]	I/O, DQ	Optional data signal for use in external memory interfacing in the x8 or x9 modes.
DM[[[0..3][L,R]],[[0..5][B,T]]]	I/O, DM	Optional data mask pins for x8/x9 modes are required when writing to DDR SDRAM and DDR2 SDRAM devices. A low signal indicates that the write is valid. If the DM signal is high, the memory masks the DQ signals. Each group of DQ & DQS signals requires a DM pin.
DM[[[1,3][L,R]],[[3,5][B,T]]][0,1]	I/O, DM	Optional data mask pins for x16/x18 modes are required when writing to DDR SDRAM and DDR2 SDRAM devices. A low signal indicates that the write is valid. If the DM signal is high, the memory masks the DQ signals. Each group of DQ & DQS signals requires a DM pin.
BWS#[[[0..3][L,R]],[[0..5][B,T]]]	I/O, BWS	Byte Write Select is an active LOW pin. When asserted active, BWS will select which byte is written into the device during write operation. Bytes not written remain unchange. Deselecting BWS will cause write data to be ignored and not written into device.
BWS#[[[1,3][L,R]],[[3,5][B,T]]][0,1]	I/O, BWS	the device during write operation. Bytes not written remain unchange. Deselecting BWS will cause write



Notes:

1. This is a top view of the silicon die.
2.This is a pictoral representation only to get an idea of placement on the device. Refer to the pin list and the Quartus II software for exact locations

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Version Number	Date	Changes Made
1.0	10/6/2004	Initial revision
1.1	2/24/2005	Modified Pin Definitions for DATA0 pin
1.2	6/2/2005	Modified Pin Type column in Pin Definitions for VREFB[1..8]N[0..1] pins
		Finalized
1.3	2/10/2005	Added footnote for pins that do not support Optional Functions (LVDS, DDR, etc)
		Added footnote for DQS0T, DQS1T, DQS0B and DQS1B pins
		Modified pin definition for NC pins
		Modified Pin Description of VREFB[1..8]N[0..1] pins
		Modified Pin Description of VCCA_PLL[1..4] and VCCD_PLL[1..4] pins
		Added Pin Description for BWS pins
1.4	3/1/2006	Added comment for PLL_OUT pins in Pin Definitions
1.5	6/16/2006	Added "I/O" to pin type of pin nCEO, nCSO and ASDO
		Moved nCEO Discription from section "Dedicated Configuration/JTAG Pins" to section "Optional/Dual-Purpose Configuration Pins"
		Modified Pin Description of VCCIO and VCCINT.
		Modified Pin Description for NCONFIG, NCE, DATA0, TMS, TCK, TDI, NSTATUS, CONDONE and DCLK pins
		Added U484 into F484 column in Pin List
		Changed Pin Name from CLK[0,2,4,6,8,10,12,14], LVDSCLK[0..7]p to CLK[0,2,4,6,9,11,13,15], LVDSCLK[0..7]p in Pin Definitions
		Changed Pin Name from CLK[1,3,5,7,9,11,13,15], LVDSCLK[0..7]n to CLK[1,3,5,7,8,10,12,14], LVDSCLK[0..7]n in Pin Definitions