Cyclone® III Device Family Pin Connection Guidelines
PCG-01003- 1.2

The pin connection guidelines are considered preliminary. These pin connection guidelines should only be used as a recommendation, not as a specification. The use of the pin connection guidelines for any particular design should be verified for device operation, with the datasheet and Altera.

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Cyclone® III Device Family Pin Connection Guidelines
PCG-01003- 1.2 *Note (1)*

You should create a Quartus® II design, enter your device I/O assignments and compile the design. Quartus II will check your pin connections with respect to I/O assignment and placement rules to ensure proper device operation. These rules are dependent on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Cyclone III Devices Pin Name	Cyclone III LS Devices Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description	Connection Guidelines
Supply and Reference Pins				
VCCINT	VCCINT	Power	These are internal logic array voltage supply pins.	All VCCINT pins must be connected to 1.2 V supply. Decoupling depends on the design decoupling requirements of the specific board. See Note 5.
VCCIO[1..8]	VCCIO[1..8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the input and output buffers for all I/O standards. VCCIO powers up the JTAG pins (TCK, TMS, TDI, and TDO) and the following configuration pins.. nCONFIG, DCLK, DATA[0..15], nCE, nCEO, nWE, nRESET, nOE, FLASH_nCE, nCSO, and CLKUSR.	Connect these pin to 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V or 3.3 V supplies, depending on the I/O standard assigned to the I/O bank. Decoupling depends on the design decoupling requirements of the specific board. See Note 5.
VREFB[1..8]N[0..2] Note 2	VREFB[1..8]N[0..2]	I/O	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard for input operation, then these pins are used as the voltage-reference pins for the bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins.	If VREF pins are not used, the designer should connect them to either the VCCIO of the I/O bank in which the pin resides or GND. Decoupling depends on the design decoupling requirements of the specific board. See Note 5. When VREF pins are used as I/O, they have higher capacitance than regular I/O pins which will slow the edge rates and affect I/O timing.
VCCA[1..4] Note 3	VCCA[1..4]	Power	Analog power for PLLs[1..4]. All VCCA pins must be powered and all VCCA pins must be powered up and powered down at the same time even if not all the PLLs are used. Designer is advised to keep isolated from other VCC for better jitter performance.	The designer must connect these pins to 2.5 V, even if the PLL is not used. These pins must be powered up and powered down at the same time. Connect VCCA[1..4] pins together. VCCA supply to the chip should be isolated. See Note 6 for details. See Note 7 for recommended decoupling.
VCCD_PLL[1..4] Note 3	VCCD_PLL[1..4]	Power	Digital power for PLLs[1..4]. The designer must power up these pins, even if the PLL is not used.	The designer must connect these pins to 1.2 V, even if the PLL is not used. Connect VCCD_PLL[1..4] pins together. VCCD_PLL supply to the chip should be isolated. See Note 6 for details. See Note 8 for recommended decoupling.
NA	VCCBAT	Power	Battery back-up power supply for design security volatile key register. The nominal voltage for this supply is 3.0 V	Connect this pin to a 3.0 V non-volatile battery power source if using the volatile key. Its valid operating range is from 1.2 to 3.3-V. When not using the volatile key tie this to either 1.8-V, 2.5-V or 3.0-V power supply.
RUP[1..4]	RUP[1..4]	I/O, Input	Reference pins for on-chip termination (OCT) block in I/O banks 2, 4, 5, and 7. The external precision resistor RUP must be connected to the designated RUP pin within the same bank when used. If the RUP pin is not used, this pin can function as a regular I/O pin.	When using OCT tie these pins to the required banks VCCIO through either a 25 Ω or 50 Ω resistor, depending on the desired I/O standard. When the device does not use this dedicated input for the external precision resistor or as an I/O, it is recommended that the pin be connected to VCCIO of the bank in which the RUP pin resides or GND.
RDN[1..4]	RDN[1..4]	I/O, Input	Reference pins for on-chip termination (OCT) block in I/O banks 2, 4, 5, and 7. The external precision resistor RDN must be connected to the designated RDN pin within the same bank when used. If the RDN pin is not used, this pin can function as a regular I/O pin.	When using OCT tie these pins to GND through either a 25 Ω or 50 Ω resistor depending on the desired I/O standard. When the device does not use this dedicated input for the external precision resistor or as an I/O, it is recommended that the pin be connected to GND.
GND	GND	Ground	Device ground pins.	All GND pins should be connected to the board GND plane.
GNDA[1..4] Note 3	GNDA[1..4]	Ground	Ground for PLLs[1..4] and other analog circuits in the device.	The designer can consider connecting the GNDA pins to the GND plane without isolating the analog ground plane on the board provided the digital GND plane(s) are stable, quiet, and with no ground bounce effect.
NC	NC	No Connect	No Connect.	Do not connect these pins to any signal. These pins should be left unconnected, except when device migration requires a different connection to support different density devices.

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PCG-01003- 1.2 *Note (1)*

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Cyclone III Devices Pin Name	Cyclone III LS Devices Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description	Connection Guidelines
Dedicated Configuration/JTAG Pins				
DCLK	DCLK	Input (PS, FPP) Output (AS, AP Note 13)	DCLK is the dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into Cyclone III device. In AS and AP Note 13 modes, DCLK is an output from the Cyclone III device that provides timing for the configuration interface.	DCLK should not be left floating. In JTAG configuration and schemes that use an external host, designer should drive it high or low, whichever is more convenient on the board. In AS and AP Note 13 mode, the DCLK has an internal pull-up resistor (typically 25-KΩ) that is always active.
DATA0	DATA0	Input (PS,FPP,AS) Bidirectional (AP Note 13)	Dedicated configuration data input pin. In serial configuration modes, bit-wide configuration data is received through this pin. In AS mode, DATA0 has an internal pull-up resistor that is always active. After AS configuration, DATA0 is a dedicated input pin with optional user control. After PS or PP configuration, DATA0 is available as a user I/O pin and the state of this pin depends on the Dual-Purpose Pin settings. After AP Note 13 configuration, DATA0 is a dedicated bidirectional pin with optional user control.	If you are using a serial configuration device in AS configuration mode, you must connect a 25-Ω series resistor at the near end of the serial configuration device for the DATA0. If DATA0 is not used, it should be driven high or low, whichever is more convenient on the board.
MSEL[0..3]	MSEL[0..3]	Input	Configuration input pins that set the Cyclone III device configuration scheme. Some of the smaller devices or package options do not support the AP Note 13 flash programming and do not have the MSEL3 pin.	These pins are internally connected to 5-KΩ resistor to GND. Do not leave these pins floating. When these pins are unused connect them to GND. Depending on the configuration scheme used, these pins should be tied to VCCA or GND. Refer to Chapter 9 of Cyclone III Device Family Handbook: Configuration, Design Security, and Remote System Upgrades in Cyclone III Devices. If only JTAG configuration is used, then connect these pins to GND.
nCE	nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.	In multi-device configuration, nCE of the first device is tied directly to GND while its nCEO pin drives the nCE of the next device in the chain. In single device configuration, nCE is tied directly to GND. The nCE pin must also be held low for successful JTAG programming of the device. If you are combining JTAG and AS configuration schemes, then the nCE should be tied to GND through a 10-KΩ resistor.
nCONFIG	nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.	If you are using PS configuration scheme with a download cable, connect this pin through a 10-KΩ resistor to VCCA. For other configuration schemes, if this pin is not used, this pin must be connected directly or through a 10-KΩ resistor to VCCIO.
CONF_DONE	CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode.	This pin is not available as a user I/O pin. CONF_DONE should be pulled high by an external 10-KΩ pull-up resistor.
nSTATUS	nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization.	This pin is not available as a user I/O pin. nSTATUS should be pulled high by an external 10-KΩ pull-up resistor.
TCK	TCK	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TCK to GND.	Connect this pin to a 1-KΩ resistor to GND.
TMS	TMS	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TMS to VCC.	When interfacing with 2.5 V/3.0 V/3.3 V configuration voltage standards, connect this pin through a 10-KΩ resistor to VCCA. For configuration voltage of 1.5 V and 1.8 V, connect this pin through a 10-KΩ resistor to VCCIO supply instead. See Note 10.

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Cyclone III Devices Pin Name	Cyclone III LS Devices Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description	Connection Guidelines
TDI	TDI	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TDI to VCC.	When interfacing with 2.5 V/3.0 V/3.3 V configuration voltage standards, connect this pin through a 10-KΩ resistor to VCCA. For configuration voltage of 1.5 V and 1.8 V, connect this pin through a 10-KΩ resistor to VCCIO supply instead. See Note 10.
TDO	TDO	Output	Dedicated JTAG output pin.	If the TDO pin is not used, leave this pin unconnected.
Clock and PLL Pins				
CLK[0,2,4,6,9,11,13,15], DIFFCLK_[0..7]p Note 4	CLK[0,2,4,6,9,11,13,15], DIFFCLK_[0..7]p	Clock, Input	Dedicated global clock input pins that can also be used for the positive terminal inputs for differential global clock input or user input pins. These dedicated clock pins do not support programmable weak pull-up resistor.	Connect unused pins to GND. See Note 9.
CLK[1,3,5,7,8,10,12,14], DIFFCLK_[0..7]n Note 4	CLK[1,3,5,7,8,10,12,14], DIFFCLK_[0..7]n	Clock, Input	Dedicated global clock input pins that can also be used for the negative terminal inputs for differential global clock input or user input pins. These dedicated clock pins do not support programmable weak pull-up resistor.	Connect unused pins to GND. See Note 9.
PLL[1..4]_CLKOUTp Note 3	PLL[1..4]_CLKOUTp	I/O, Output	Optional positive terminal for external clock outputs from PLL [1..4]. These pins can be assigned to single-ended or differential I/O standards if it is being fed by a PLL output.	Connect unused pins to GND. See Note 9.
PLL[1..4]_CLKOUTn Note 3	PLL[1..4]_CLKOUTn	I/O, Output	Optional negative terminal for external clock outputs from PLL[1..4]. These pins can be assigned to single-ended or differential I/O standards if it is being fed by a PLL output.	Connect unused pins to GND. See Note 9.
Optional/Dual-Purpose Configuration Pins				
nCEO	nCEO	I/O, Output (open-drain)	Output that drives low when device configuration is complete.	During multi-device configuration, this pin feeds a subsequent device's nCE pin and must be pulled high to VCCIO by an external 10-KΩ pull-up resistor. During single device configuration and for the last device in multi-device configuration, this pin can be left floating or used as a user I/O after configuration.
FLASH_nCE, nCSO	nCSO	I/O, Output(AS, AP Note 13)	This pin functions as FLASH_nCE in AP Note13 mode, and nCSO in AS mode. This pin has an internal pull-up resistor that is always active. nCSO: Output control signal from the Cyclone III device to the serial configuration device in AS mode that enables the configuration device. FLASH_nCE: Output control signal from the Cyclone III device to the parallel flash in AP Note 13 mode that enables the flash.	When not programming the device in AS mode, nCSO is not used. Similarly, FLASH_nCE is not used when not programming the device in AP Note 13 mode. If the pin is not used as an I/O then it is recommended to leave the pin unconnected.
DATA1, ASDO	DATA1, ASDO	Input (FPP) Output (AS) Bidirectional (AP Note 13)	This pin functions as DATA1 in PS and FPP modes, and as ASDO in AS mode. DATA1: Data input in non-AS mode. Byte-wide or word-wide configuration data is presented to the target device on DATA[0..7] or DATA[0..15] respectively. In PS configuration scheme, DATA1 functions as user I/O pin during configuration, which means it is tri-stated. After FPP configuration, DATA1 is available as a user I/O pin and the state of this pin depends on the Dual-Purpose Pin settings. ASDO: Control signal from the Cyclone III device to the serial configuration device in AS mode used to read out configuration data. In AS mode, this ASDO pin has an internal pull-up resistor that is always active. After AS configuration, this pin is a dedicated output pin with optional user control.	When not programming the device in AS mode, this pin is available as a user I/O pin. If the pin is not used as an I/O then it is recommended to leave the pin unconnected.

Cyclone® III Device Family Pin Connection Guidelines
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Cyclone III Devices Pin Name	Cyclone III LS Devices Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description	Connection Guidelines
DATA[2..7]	DATA[2..7]	Inputs (FPP) Bidirectional (AP Note 13)	Data inputs. Byte-wide or word-wide configuration data is presented to the target device on DATA [0..7] or DATA [0..15] respectively. In AS or PS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated. After FPP configuration, DATA [2..7] are available as user I/O pins and the state of these pins depends on the Dual-Purpose Pin settings.	When not programming the device in AS mode, this pin is available as a user I/O pin. If the pin is not used as an I/O then it is recommended to tie this pin to VCCIO, GND, or leave the pin unconnected.
DATA[8..15]	NA	Bidirectional (AP Note 13)	In the PS, FPP, or AS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated. After AP Note 13 configuration, DATA[8..15] are dedicated bidirectional pins with optional user control.	When not programming the device in AP Note 13 mode, these pins are available as user I/O pins. If these pins are not used as I/Os, then it is recommended to tie this pin to VCCIO, GND, or leave the pin unconnected.
PADD[0..23]	NA	Output (AP Note 13)	24-bit address bus from the Cyclone III device to the parallel flash in AP Note 13 mode.	When not programming the device in AP Note 13 mode, these pins are available as user I/O pins. If these pins are not used as I/Os, then it is recommended to tie this pin to VCCIO, GND or leave the pin unconnected.
nRESET	NA	Output (AP Note13)	Active-low reset output. Driving the nRESET pin low resets the parallel flash.	When not programming the device in AP Note 13 mode, nRESET is not used and is available as a user I/O pin. If the pin is not used as an I/O then it is recommended to tie this pin to VCCIO, GND or leave the pin unconnected.
nAVD	NA	Output (AP Note 13)	Active-low address valid output. Driving the nAVD pin low during read or write operation indicates to the parallel flash that valid address is present on the PADD[0..23] address bus.	When not programming the device in AP Note 13 mode, nAVD is not used and is available as a user I/O pin. If the pin is not used as an I/O then it is recommended to tie this pin to VCCIO, GND or leave the pin unconnected.
nOE	NA	Output (AP Note 13)	Active-low output enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash outputs (DATA[0..15] and RDY).	When not programming the device in AP Note 13 mode, nOE is not used and is available as a user I/O pin. If the pin is not used as an I/O then it is recommended to tie this pin to VCCIO, GND or leave the pin unconnected.
nWE	NA	Output (AP Note 13)	Active-low write enable to the parallel flash. Driving the nWE pin low during write operation indicates to the parallel flash that data on the DATA[0..15] bus is valid.	When not programming the device in AP Note 13 mode, nWE is not used and is available as a user I/O pin. If the pin is not used as an I/O then it is recommended to tie this pin to VCCIO, GND, or leave the pin unconnected.
RDY	NA	Output (AP Note13)	Control signal (WAIT) from the parallel flash is connected to this pin in the Cyclone III device to indicate when synchronous data is ready on the data bus.	The current implementation for AP Note 13 configuration ignores the RDY pin. However it is highly recommended to connect this pin to the AP Note 13 flash.
CRC_ERROR	CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.	When the CRC error detection circuitry is disabled and when this pin is not used as an I/O then it is recommended to tie this pin to VCCIO, GND or leave the pin unconnected.
DEV_CLRn	DEV_CLRn	I/O (when option off), Input (when option on)	Optional chip-wide reset pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. The DEV_CLRn pin does not affect JTAG boundary-scan or programming operations. This pin is enabled by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus II software.	When the input DEV_CLRn is not used and this pin is not used as an I/O then it is recommended to tie this pin to VCCIO, GND, or leave the pin unconnected.
DEV_OE	DEV_OE	I/O (when option off), Input (when option on)	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.	When the input DEV_OE is not used and this pin is not used as an I/O then it is recommended to tie this pin to VCCIO, GND, or leave the pin unconnected.

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INIT_DONE	INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose status pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software.	Connect this pin to a 10-KΩ resistor to VCCIO.
CLKUSR	CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software.	If the CLKUSR pin is not used as a configuration clock input and the pin is not used as an I/O then it is recommended to connect this pin to GND.
Dual-Purpose Differential & External Memory Interface Pins				
DIFFIO_[L,R,T,B][0..61][n,p] Note 11	DIFFIO_[L,R,T,B][0..47][n,p] Note 11	I/O, TX/RX channel	Dual-purpose differential transmitter/receiver channels. These channels can be used for transmitting/receiving LVDS compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	When these I/O pins are not used they can be tied to the VCCIO of the bank they reside in or GND. See Note 9.
DQS[0..5][L,R,T,B]/CQ[1,3,5][L,R,T,B][#],DPCLK[0..11] Note 12	DQS[0..5][L,R,T,B]/CQ[1,3,5][L,R,T,B][#],DPCLK[0..11] Note 12	I/O, DQS/CQ,DPCLK	Dual-purpose DPCLK/DQS pins can connect to the global clock network for high fan-out control signals such as clocks, asynchronous clears, presets and clock enables. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry, which allows fine tune of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.	When these I/O pins are not used they can be tied to the VCCIO of the bank they reside in or GND. See Note 9.
DQS[0..5][L,R,T,B]/CQ[1,3,5][L,R,T,B][#],CDPCLK[0..7] Note 12	DQS[0..5][L,R,T,B]/CQ[1,3,5][L,R,T,B][#],CDPCLK[0..7] Note 12	I/O, DQS/CQ,CDPCLK	Dual-purpose CDPCLK/DQS pins can connect to the global clock network for high fan-out control signals such as clocks, asynchronous clears, presets, and clock enables. Only one of the two CDPCLK in each corner can feed the clock control block at a time. The other pin can be used as general-purpose I/O pin. The CDPCLK signals incur more delay to the clock block control because they are multiplexed before driving into the clock block control. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry, which allows fine tune of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.	When these I/O pins are not used they can be tied to the VCCIO of the bank they reside in or GND. See Note 9.
DQ[0..5][L,R,T,B] Note 12	DQ[0..5][L,R,T,B][0..35] Note 12	I/O, DQ	Optional data signal for use in external memory interface.	When these I/O pins are not used they can be tied to the VCCIO of the bank they reside in or GND. See Note 9.
DM[0..5][L,R,B,T][0..1]/BWS#[0..5][L,R,T,B]	DM[0..5][L,R,B,T][0..1]/BWS#[0..5][L,R,T,B][0..3]	I/O, DM/BWS#	The data mask pins are only required when writing to DDR SDRAM and DDR2 SDRAM devices. QDRII SRAM devices use the BWS signal to select the byte to be written into memory. A low signal on the DM/BWS# pin indicates that the write is valid. Driving the DM/BWS# pin high results in the memory masking the DQ signals.	When these I/O pins are not used they can be tied to the VCCIO of the bank they reside in or GND. See Note 9.

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Pins Used to Turn On the Security Boundary Between I/O Banks				
NA	B1 Note 14	I/O, Power, Ground	Pins used for setting up the security boundary for TDI, TDO and DATA0.	To guarantee physical I/O separation of the JTAG, B1 labeled I/O pins should be connected to GND. Other B1 labeled pin such as VCCIO and GND pins should remain their initial function i.e VCCIO pin should remain connected to the power supply and GND pin should remain connected to ground.
NA	B1_B2, B2_B3, B3_B4, B4_B5, B5_B6, B6_B7, B7_B8, B8_B1 Note 15	I/O, Power, Ground	Physical pins that are used to turn on the security boundary between the I/O banks that is specified. For example: B1 for Bank 1 and B2 for Bank 2.	When the I/O pins are used to turn on the security boundary between the I/O banks, the I/O pins must be connected to GND. The VCCIO and GND pins used to turn on the security boundary between the I/O banks should remain their initial function i.e VCCIO pin should remain connected to the power supply and GND pin should remain connected to ground.

Legend:

Shaded cells indicate pins that are used in AP configuration mode for Cyclone III Devices and other configuration modes (except AP configuration mode) in Cyclone III LS Devices.

Notes:

(1) This pin connection guideline is created based on the largest device density that is EP3C120F780 for Cyclone III Devices and EP3CLS200F780 for Cyclone III LS Devices.
(2) EP3C5 and EP3C10 only support VREFB[1..8]N0.
(3) EP3C5 and EP3C10 only have PLL(1 & 2). EP3C16 and other larger densities have PLL (1,2,3, and 4).
(4) The number of dedicated global clocks for each device density is different. EP3C5 and EP3C10 support four dedicated clock pins on the left and right sides of the device, that can drive a total of 10 global clock networks. EP3C16 and other larger densities support four dedicated clock pins on each side of the device that can drive a total of 20 global clock networks.

(5) Capacitance values for the power supply decoupling capacitors should be selected after consideration of the amount of power needed to supply over the frequency of operation of the particular circuit being decoupled. A target impedance for the power plane should be calculated based on current draw and voltage drop requirements of the device/supply. The power plane should then be decoupled using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to “Equivalent Series Inductance” of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling. To assist in decoupling analysis, Altera's "Power Distribution Network (PDN) Design Tool" serves as an excellent decoupling analysis tool. The PDN design tool can be obtained at

Power Distribution Network Design Tool.

(6) Use seperate power island for VCCA and VCCD_PLL. PLL power supply may originate from another plane on the board but must be isolated using a ferrite bead or other equivalent methods. If using a ferrite bead, choose an 0402 package with low DC resistance, higher current rating than the maximum steady state current for the supply it is connected to(VCCA or VCCD_PLL) and high impedance at 100 MHz.

(7) The VCCA power island can be decoupled with a combination of decoupling capacitors. Please refer to the

Power Distribution Network Design Tool

to determine the decoupling capacitors value. Use 0402 package for 0.1 uF and smaller capacitors for lower mounting inductance. Place 0.1 uF and smaller capacitors as close to the device as possible. On-board capacitors do not decouple higher than 100 MHz due to “Equivalent Series Inductance” of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling. To minimize impact on jitter, a 20 mV ripple voltage was used in the analysis for VCCA decoupling. Refer to Figure <1> for decoupling capacitor placement guidelines. Figure <1> depicts symbolic representation of decoupling scheme and not the exact layout.

(8) The VCCD_PLL power island can be decoupled with a combination of decoupling capacitors. Please refer to the “Power Distribution Network Design Tool” at

Power Distribution Network Design Tool

to determine the decoupling capacitors value. Place 0.1 uF and smaller capacitors as close to the device as possible. On-board capacitors do not decouple higher than 100 MHz due to “Equivalent Series Inductance” of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling. To minimize impact on jitter, a 20 mV ripple voltage was used in the analysis for VCCD_PLL decoupling. Refer to Figure <1> for decoupling capacitor placement guidelines. Figure <1> depicts symbolic representation of decoupling scheme and not the exact layout.

(9) The unused pins must be connected as specified in the Quartus II software settings. The default Quartus II setting for unused pins is 'As inputs tri-stated with weak pull-up resistors', unless for specific pins that Quartus II software connects them to GND automatically. To change the setting, go to 'Assignments', then 'Device'. Click on 'Device & Pin options' dialog box and go to 'Unused Pins' tab. You may choose the desired setting from the 'Reserve all unused pins' drop down list.

(10) You must follow specific requirements when interfacing Cyclone III device with 2.5 V/3.0 V/3.3 V configuration voltage standards. All I/O inputs must maintain a maximum AC voltage of 4.1 V. Refer to Configuration and JTAG Pin I/O Requirements of Chapter 9: Configuration, Design Security, and Remote System Upgrades in Cyclone III Devices.

(11) The differential TX/RX channels for each device density and package is different. Please refer to the Cyclone III Device Family Handbook Chapter 7. High-Speed Differential Interfaces in Cyclone III Devices.

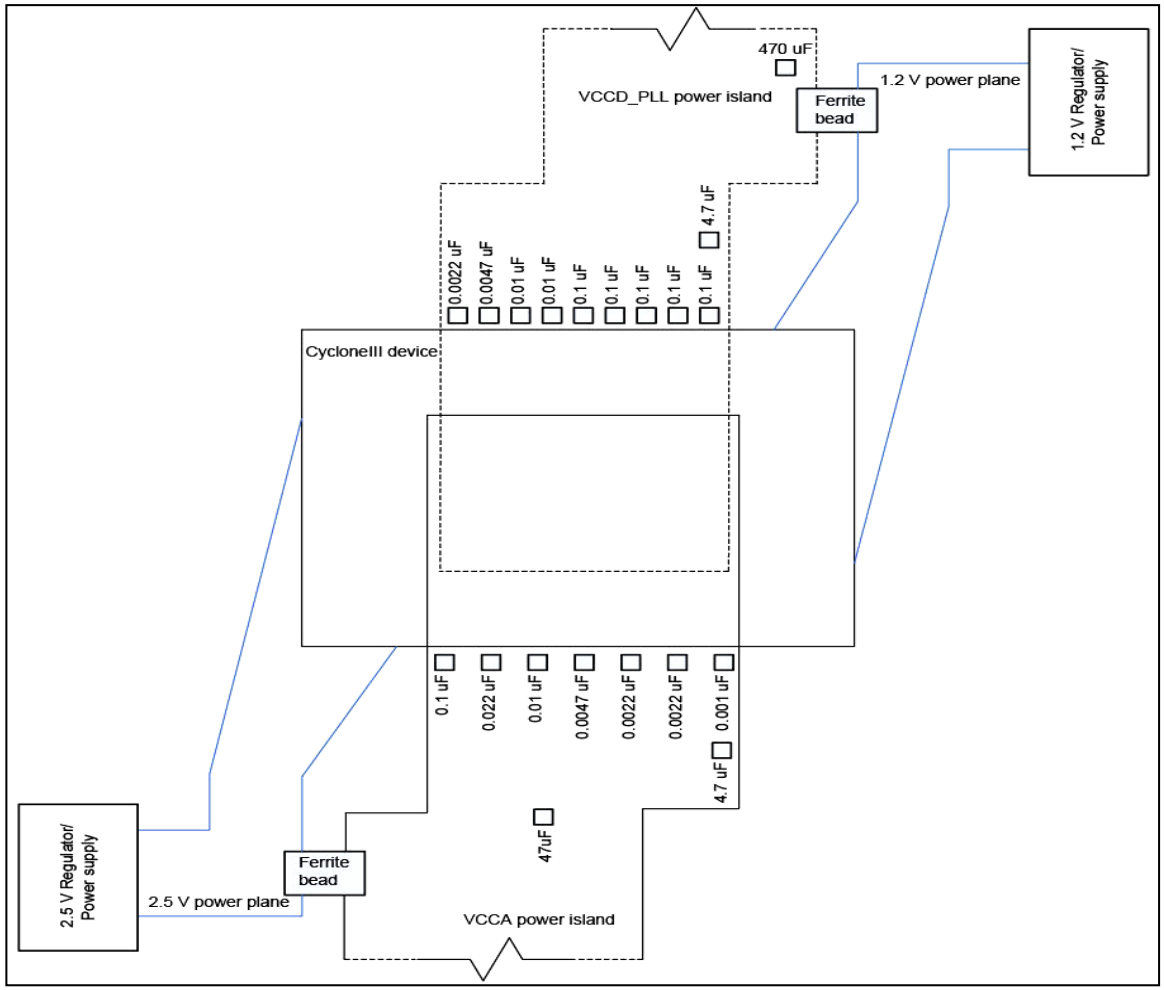
(12) For details about the DQ and DQS bus modes support in different device densities, refer to the Cyclone III Device Family Handbook Chapter 8. External Memory Interfaces in Cyclone III Devices.

(13) Configuration in AP mode is only supported in Cyclone III Devices and not in Cyclone III LS Devices.

(14) B1 is not the pin name in the Cyclone III LS Device family but rather the labeled named used for the I/O, power and ground pins used to form the security boundary for TDI, TDO, and DATA0 pin. Please refer to Cyclone III LS Devices Pin-out file for more information.

(15) B1_B2, B2_B3, B3_B4, B4_B5, B5_B6, B6_B7, B7_B8, B8_B1 are not the pin name in the Cyclone III LS Device family but rather the labeled name used for I/O, power, or ground pins used to form the security boundary to separate the banks. Please refer to the Cyclone III LS Devices Pin-out files for more information.

Figure 1: PLL Power Decoupling Diagram



Cyclone® III Device Family Pin Connection Guidelines PCG-01003- 1.2		
Version Number	**Date**	**Changes Made**
1.0	10/17/2007	Initial release to Altera Literature site.
1.1	6/22/2009	Updated to include Cyclone III LS device connection guidelines.
1.2	4/30/2014	Updated the pin type for DATA0 and DATA1 pins.