



# Nios II Performance Benchmarks



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# 1 Nios® II Performance Benchmarks

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## 1.1 Performance Benchmarks Overview

This datasheet lists the performance and logic element (LE) usage for a typical implementation of a Nios® II soft processor and peripherals. Nios II processors are configurable and designed for implementation in Intel® FPGAs. The following Nios II processors cores were used for these benchmarks:<sup>(1)</sup>

- Nios II/f—The Nios II/f “fast” processor is designed for high performance and has the most configuration options, some of which are unavailable in the Nios II/e processor.
- Nios II/e—The Nios II/e “economy” processor is designed for the smallest possible logic size while still providing adequate performance.

The default options for the Nios II processor were chosen for these benchmarks, unless specified otherwise.

*Note:* Results may vary slightly depending on the version of the Intel Quartus® Prime software, the version of the Nios II processor, compiler version, target device and the configuration of the processor. Also, any changes to the system logic design might change the performance and LE usage. All results are generated from designs built using the Platform Designer tool.

The Dhrystone MIPS (DMIPS) reports were obtained using the Dhrystone 2.1 benchmark. You can download the Dhrystone 2.1 benchmark software with the **Fast Nios II Hardware Design Example** on the Intel FPGA website. For more information about the Dhrystone 2.1 benchmark software and the Fast design example, refer to the **readme.txt** file which is included in the design example page.

The CoreMark software can be registered and downloaded at [www.eembc.org](http://www.eembc.org).

*Note:* The Nios II Classic and Nios II benchmark data are very similar. The Nios II processor was used to create the systems which gave the data values reported in this document. Please refer to the older versions of this document for values associated with the Classic cores.

The resource utilization results were generated using moderate Analysis, Synthesis and Fitter settings in the Quartus Prime software. These results represent typical results.

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<sup>(1)</sup> The Nios II/s core is only available with the Nios II Classic soft processor.



**Table 1. System Configuration for Nios II Performance Benchmarks**

Benchmark	Nios II Processor	I-Cache	D-Cache	Other options	Peripherals
f <sub>max</sub>	Nios II/f	4 Kbytes	2 Kbytes	<ul style="list-style-type: none"> <li>JTAG debug module (default)</li> <li>Hardware multiplier</li> </ul>	<ul style="list-style-type: none"> <li>64 Kbytes On-chip RAM</li> <li>Avalon Memory-Mapped pipeline Bridge</li> <li>JTAG UART</li> <li>Timer</li> </ul>
	Nios II/e	None	None	<ul style="list-style-type: none"> <li>JTAG debug module (default)</li> </ul>	<ul style="list-style-type: none"> <li>64 Kbytes On-chip RAM</li> <li>Avalon Memory-Mapped pipeline Bridge</li> <li>JTAG UART</li> <li>Timer</li> </ul>
Logic size	Nios II/f	4 Kbytes	2 Kbytes	<ul style="list-style-type: none"> <li>JTAG debug module (default)</li> <li>Hardware multiplier</li> </ul>	<ul style="list-style-type: none"> <li>64 Kbytes On-chip RAM</li> <li>Avalon Memory-Mapped pipeline Bridge</li> <li>JTAG UART</li> <li>Timer</li> <li>Avalon UART</li> <li>SDRAM controller<sup>(3)</sup></li> </ul>
	Nios II/e	None	None	<ul style="list-style-type: none"> <li>JTAG debug module (default)</li> </ul>	<ul style="list-style-type: none"> <li>64 Kbytes On-chip RAM</li> <li>Avalon Memory-Mapped pipeline Bridge</li> <li>JTAG UART</li> <li>Timer</li> <li>Avalon UART</li> <li>SDRAM controller<sup>(3)</sup></li> </ul>
DMIPS	Nios II/f at 100 MHz	4 Kbytes	2 Kbytes	<ul style="list-style-type: none"> <li>JTAG debug module (default)</li> <li>Hardware multiplier</li> </ul>	<ul style="list-style-type: none"> <li>128 Kbytes On-chip RAM</li> <li>JTAG UART</li> <li>Timer</li> </ul>
	Nios II/e at 100 MHz	-	-	<ul style="list-style-type: none"> <li>JTAG debug module (default)</li> </ul>	<ul style="list-style-type: none"> <li>128 Kbytes On-chip RAM</li> <li>JTAG UART</li> <li>Timer</li> </ul>
CoreMark <sup>(2)</sup>	Nios II/f at 100 MHz	32 Kbytes	32 Kbytes	<ul style="list-style-type: none"> <li>JTAG debug module (default)</li> <li>Hardware multiplier</li> </ul>	<ul style="list-style-type: none"> <li>128 Kbytes On-chip RAM</li> <li>JTAG UART</li> <li>Timer</li> </ul>
	Nios II/e at 100 MHz	-	-	<ul style="list-style-type: none"> <li>JTAG debug module (default)</li> </ul>	<ul style="list-style-type: none"> <li>128 Kbytes On-chip RAM</li> <li>JTAG UART</li> <li>Timer</li> </ul>

**Related Links**

- [Fast Nios II Hardware Design Example](#)
- [CoreMark Software Download](#)

<sup>(2)</sup> This benchmark is compiled with the gcc -o3 switch for optimised performance.

<sup>(3)</sup> The RAM controller for the device is based on DDR3 SDRAM Controller with UniPHY. For Intel Cyclone® 10, Intel Arria® 10, and Intel Stratix® 10 devices, the RAM controller is based on the respective device IP.



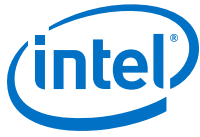
### 1.1.1 Nios II Performance Benchmarks

Table 2.  $f_{\max}$  for Nios II Processor System (MHz)

Device Family	Device used	Nios II/f <sup>(4)</sup>	Nios II/e <sup>(4)</sup>
Intel Stratix 10	1SG250LN3F43I2LG	320	340
Stratix V	5SGXEA7N2F45C1	330	400
Stratix IV	EP4S100G5H40I1	240	270
Intel Arria 10	10AX115U3F45I2LG	290	340
Arria V GZ	5AGZME7K2F40C3	280	360
Arria V	5AGXFB5K4F40I3	210	250
Intel Cyclone 10 GX	10CX220YF780E5G	290	330
Intel Cyclone 10 LP	10CL120YF780I7G	130	160
Cyclone V	5CGXFC7D6F31C6	170	230
Cyclone IV	EP4CGX30CF19C6	150	170
Intel MAX® 10	10M50DAF484C6GES	140	160

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(4) Results were generated using the analysis, synthesis and fitter settings in Intel Quartus Prime.



**Table 3. Typical Logic Size for Nios II Processor Cores and Peripherals**

Device Family	Processor Core / Peripheral						
	Nios II/f	Nios II/e	Nios II JTAG debug module	Avalon UART	JTAG UART	SDRAM Controller <sup>(5)</sup>	Timer
Intel Stratix 10 (ALM)	1229	618	174	64	79	4946	80
Stratix V (ALM)	724	295	129	61	56	2629	68
Stratix IV (ALUT)	1137	527	169	95	112	3805	92
Intel Arria 10 (ALM)	849	292	114	56	59	4175	57
Arria V GZ (ALM)	732	287	126	56	57	2627	55
Arria V (ALM)	845	308	124	56	57	2472	55
Intel Cyclone 10 GX (ALM)	984	462	118	56	60	933	146
Intel Cyclone 10 LP (LE)	2387	845	459	56	60	2528	57
Cyclone V (ALM)	858	305	124	56	59	2470	56
Cyclone IV GX (ALUT)	2259	768	357	142	159	423	138
Intel MAX 10 (LE)	2265	795	368	139	159	4659	136

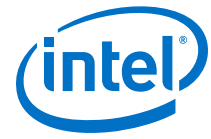
**Table 4. Nios II Processor Architecture Performance**

Performance Metric	Nios II/f	Nios II/e
DMIPS/MHz Ratio	0.9	0.1
CoreMark	224.7	19

**Related Links**

- [AN-440: Accelerating Nios II Networking Applications](#)  
For more information about the Nios II networking applications performance.
- [Nios II Custom Instruction User Guide](#)  
For more information about the Nios II floating-point custom instruction performance.
- [Embedded Design Handbook](#)  
For more information about the Nios II Configuration and Booting Solutions.

<sup>(5)</sup> The RAM controller for the device is based on DDR3 SDRAM Controller with UniPHY. For Intel Cyclone 10, Intel Arria 10, and Intel Stratix 10 devices, the RAM controller is based on the respective device IP.



## 1.2 Document Revision History

**Table 5. Document Revision History**

Version	Changes
2017.12.18	<ul style="list-style-type: none"><li>• Updated for Intel Quartus Prime 17.1 version.</li><li>• Added the Intel Cyclone 10 GX, and Intel Stratix 10 results.</li></ul>
2017.06.12	<ul style="list-style-type: none"><li>• Updated for Intel Quartus Prime 17.0 version.</li><li>• Added the Intel Cyclone 10 LP results.</li></ul>
2016.06.24	<ul style="list-style-type: none"><li>• Updated for Intel Quartus Prime 16.0 version.</li><li>• Added the Cyclone IV results.</li></ul>
2015.12.16	<ul style="list-style-type: none"><li>• Updated for Intel Quartus Prime 15.1 version.</li><li>• Added the Intel Arria 10 and CoreMark results.</li></ul>