Cyclone II FPGA Family

ES-030405-1.3 Errata Sheet

Introduction

This errata sheet provides updated information on Cyclone™ II devices. This document addresses known device issues and includes methods to work around the issues.

Table 1 shows the specific issues and which Cyclone II devices each issue affects.

Table 1. Cyclone II FPGA Family Issue

Issue	Affected Devices	Fixed Devices
JTAG TDO output pin will drive out logic high for all user-mode, non-shift JTAG states (RUN_TEST/IDLE, CAPTURE_DR, PAUSE_IR, etc.) when it should be inactive or tri-state during these states.	EP2C35 Revision A	EP2C35 Revision B and later
M4K block write operations may fail in certain memory modes and configurations.	EP2C35 Revision A and B EP2C5, EP2C8, EP2C20, EP2C50, EP2C70 Revision A *(1)*	EP2C35 Revision C and later EP2C5, EP2C8, EP2C20, EP2C50, EP2C70 Revision B and later *(2)*

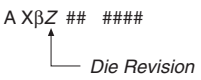
Notes to Table 1:

(1) Altera offers permanent workarounds for specific memory modes and configurations for affected devices. Refer to "M4K Memory Block Write Issue" on page 2 for more information.

(2) Designs targeting fixed devices need to be compiled in the Quartus II software version 5.1 SP2 or later for correct functionality and performance. Refer to "Fixed Devices Information" on page 9 for more information.

The die revision is identified by the alphanumeric character (Z) before the fab code (first two alphanumeric characters) in the date code printed on the top side of the device. Figure 1 shows a Cyclone II device's top side date code.

Figure 1. Cyclone II Device Top Side Lot Number



EP2C35 JTAG TDO Output Issue

Altera has identified a silicon issue affecting Cyclone II EP2C35 Revision A devices. This issue is fixed in Revision B and later devices. The problem affects the JTAG TDO pin in user mode (after configuration) only.

The EP2C35 Revision A device JTAG TDO output pin will drive out logic high for all non-shift JTAG states (RUN_TEST/IDLE, CAPTURE_DR, PAUSE_IR, etc.) when it should be inactive or tri-state during these states. The TDO output behaves correctly for shift states (SHIFT_IR and SHIFT_DR), driving out data according to the selected instruction or data register.

This problem does not affect JTAG configuration in either a single-device or multi-device JTAG chain. The TDO pin functions properly before and during configuration as well as in SHIFT_IR or SHIFT_DR states regardless of whether the device has been configured.

This issue affects board designs that use parallel connected JTAG test paths after configuration rather than standard serial connections. Designs that use a parallel JTAG test path must use fixed silicon devices.

M4K Memory Block Write Issue

Altera has identified a write issue when using M4K blocks in certain memory modes and configurations. M4K blocks utilizing dual clock mode in FIFO, simple dual-port, and true dual-port modes may exhibit a write failure when there is a specific phase relationship between the two clocks.

Table 2 lists the effects of this issue on the M4K operation in different modes for all Cyclone II devices.

Table 2. M4K Safe Operation Modes for All Devices

M4K Mode	Safe Mode
ROM	Always safe
Single port	Always safe
Single clock FIFO, simple or true dual port	Always safe
Dual clock FIFO, simple or true dual port	At risk. Use the Quartus II software version 5.0 SP2 or later to remap affected memory blocks into a safe mode to generate programming files. Refer to Table 3 for more details.

Designs targeting both affected and fixed devices must utilize the Quartus® II workaround to avoid write failures. Designs targeting only fixed devices do not require the workaround and will not be compatible with affected devices. Refer to "Fixed Devices Information" on page 9 for more information.

Quartus II Workaround

The Quartus II software version 5.0 SP2 and later provides a permanent workaround to address most M4K configurations identified as "at risk." The Quartus II software remaps such memory configurations to avoid modes that are at risk. Table 3 lists the effects of the permanent workaround for the various M4K modes.

Table 4 describes the action taken by the Quartus II software to remap the memory blocks and the resulting design impact. The performance impact from the action is design-dependent and will require designers to compile their designs and refer to the Timing Analysis Report to get an accurate assessment.

Designs compiled using the Quartus II software version 5.0 SP2 or later are robust and will not exhibit the write failures under any conditions.

Table 3. M4K Workaround Description (Part 1 of 2)

RAM Mode	Clock Mode	Port A / Write Width	Port B / Read Width	Number of Words	Configuration Option Used					Quartus II Software Action *(1)*
					Read Enable	Address Stall	Clock Enable (Read)	Byte Enable	Q Output Register	
ROM	All	Any	Any	Any	n/a	*(2)*	*(2)*	*(2)*	*(2)*	None
Single port	All	Any	Any	Any	n/a	*(2)*	*(2)*	*(2)*	*(2)*	None
Simple dual port (FIFO)	Single clock	Any	Any	Any	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	None
	Input/ output	Any	Any	Any	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	None
	Read/ write	A = B	A = B	≤128	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	None
		×1	×32	Any	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	None
		×2, ×4, ×8, ×16	×32	≤128	*(2)*	*(2)*	*(2)*	N *(3)*	*(2)*	None
		×9, ×18	×36	≤128	*(2)*	*(2)*	*(2)*	N *(3)*	*(2)*	None
		(5)	*(5)*	Any	N *(3)*	*(2)*	*(2)*	*(2)*	*(2)*	Port swap
		(5)	*(5)*	Any	*(2)*	N *(3)*	N *(3)*	*(2)*	N *(3)*	Port swap
		(5)	*(5)*	Any	Y *(4)*	Y *(4)*	Y *(4)*	*(2)*	Y *(4)*	Read enable emulation
		×32	×1	Any	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	Bit multiplexing
		×32	×2, ×4, ×8, ×16	≤128	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	Bit multiplexing
		×36	×9, ×18	≤128	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	Bit multiplexing

Table 3. M4K Workaround Description (Part 2 of 2)

RAM Mode	Clock Mode	Port A / Write Width	Port B / Read Width	Number of Words	Configuration Option Used					Quartus II Software Action *(1)*
					Read Enable	Address Stall	Clock Enable (Read)	Byte Enable	Q Output Register	
True dual port	Single clock	Any	Any	Any	n/a	*(2)*	*(2)*	*(2)*	*(2)*	None
	Input/ output	Any	Any	Any	n/a	*(2)*	*(2)*	*(2)*	*(2)*	None
	Clk A/ Clk B	Any	Any	Any	n/a	*(2)*	*(2)*	*(2)*	*(2)*	True dual port *(6)*
		A ≠ B	A ≠ B	Any	n/a	*(2)*	*(2)*	Y *(4)*	*(2)*	n/a *(6)*

Notes to Table 3:
(1) For a description of the design impact from the Quartus II software action, see Table 4.
(2) This configuration option can be on or off.
(3) This configuration option cannot be used and must be turned off.
(4) This configuration option is used and must be turned on.
(5) Any A/B width ratio other than 32:1 or 1:32
(6) Refer to "Special Cases" on page 8 for more information

Table 4. Quartus II Workaround Remapping Method & Impact

Quartus II Software Action	Effect			
	f_{MAX}	t_{CO}	LE Usage	M4K Usage
No change	None	None	None	None
Port swap	None	None	None	None
Read enable emulation	Small decrease	None	Small increase	None
Bit multiplexing	Decrease	Increase	Increase	None
True dual port	Small decrease	Small increase	Small increase	2× increase

CYCLONEII_SAFE_WRITE Parameter

Designers must set the `CYCLONEII_SAFE_WRITE` parameter for memory configurations that require the Quartus II software to remap the design. If the parameter is not set correctly, the compilation will result in an error.

Use the following steps to set the `CYCLONEII_SAFE_WRITE` parameter globally:

1. From the Assignments menu, click **Settings**.

2. Under Analysis & Synthesis, select **Default Parameters**.

3. Enter the desired parameters.

Designers can make an assignment to a specific entity in the Assignment Editor to affect only that entity. Figures 2 and 3 show where to make the parameter assignment in the Quartus II software.

Figure 2. Setting CYCLONEII_SAFE_WRITE Parameter Globally

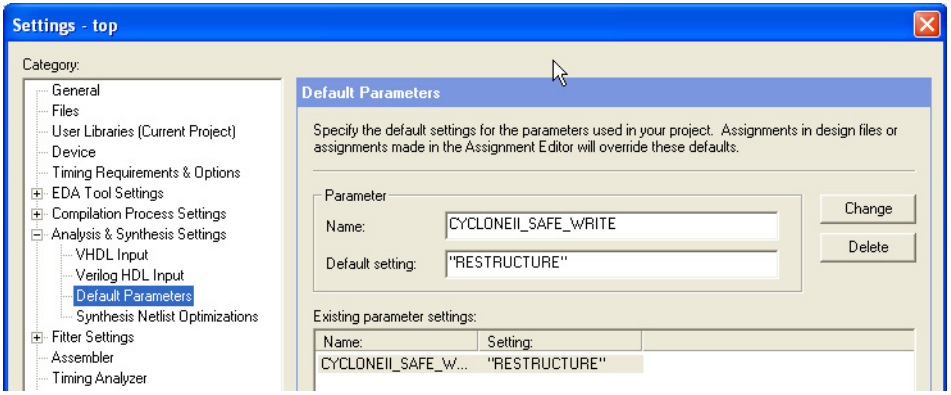


Figure 3. Setting CYCLONEII_SAFE_WRITE Parameter for a Specific Entity

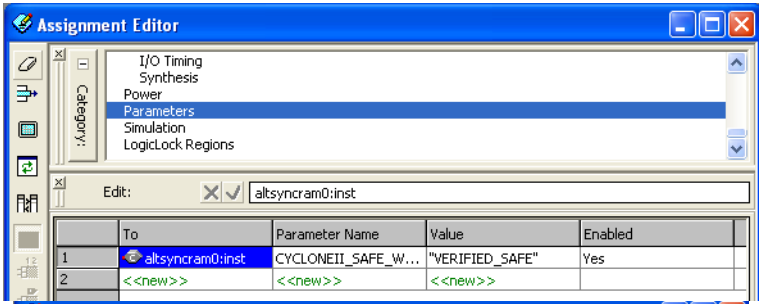


Table 5 describes the CYCLONEII_SAFE_WRITE parameter values.

Table 5. CYCLONEII_SAFE_WRITE Parameter

Value	Action
NO_CHANGE	No memory blocks will be modified. The Quartus II software issues an error for memory blocks in un-safe modes.
PORT_SWAP (default)	Only changes memory blocks that will have no design impact (port swap remapping methods). The Quartus II software issues an error for memory blocks that require read enable emulation, bit multiplexing, or true dual port remapping methods.
RESTRUCTURE	Remap all memory blocks (port swap, read enable emulation, bit multiplexing, and true dual port remapping methods).
VERIFIED_SAFE	User has verified memory block to be safe. The Quartus II software will issue a warning for memory blocks in unsafe modes.

To allow any RAM configuration to go through the Quartus II software unchanged, set the CYCLONEII_SAFE_WRITE parameter to VERIFIED_SAFE. This setting allows the Quartus II software to bypass any legality checking and implement the memory blocks in the default mode, without modifications.

The CYCLONEII_SAFE_WRITE parameter will correctly handle designs using inferred memories and memories instantiated directly without using the MegaWizard® Plug-In Manager.

The CYCLONEII_SAFE_WRITE parameter does not support the **Generate clear box netlist file instead of a default wrapper file (for use with supported EDA synthesis tools only)** option. If this option is set to **On**, the Quartus II software will ignore the CYCLONEII_SAFE_WRITE parameter and issue an error.

If the design contains a Verilog Quartus Mapping File **(.vqm)** with memory block instantiations, setting the parameter will not affect the design. An error will be issued stating that the memory block is in an unsafe mode. The VQM netlist needs to be regenerated with the appropriate parameter using Quartus II software version 5.0 SP2 or later.

All Cyclone II designs using M4K blocks need to be recompiled in Quartus II software version 5.0 SP2 or later to function correctly.

Special Cases

This section provides information for several special M4K configuration cases. The Quartus II software does not automatically address these cases, and they require action by the designer.

TDP Mode, Dual-Clock, Mixed-Width Ports with Byte Enable

When using true dual-port mode with dual clocks using byte enable with mixed port widths (for example, Port A width not equal to Port B width) the Quartus II compilation may result in an error.

The Quartus II software is able to handle some cases of the mixed-width byte-enable configurations. It will depend on the configuration of the memory and the choices available to the Quartus II software Fitter. For cases that result in a successful compile, the Quartus II software will implement the **True dual port** action which will result in a 2 × increase in the M4K block usage. However, for cases that result in an error during compilation, there is no workaround and the designer must use fixed silicon to implement this configuration.

Refer to Table 1 for a list of fixed devices.

TDP Mode, Dual-Clock, Read/Write on Port B, Read on Port A

When using true dual-port mode with dual clocks where port B is used for read and write operations and port A is used only for read operations, the design can safely use the default memory mapping. If the `wren_a` port is connected to GND, set the `CYCLONEII_SAFE_WRITE` parameter to `NO_CHANGE`. If the designer can guarantee the design will never assert the `wren_a` control signal, set the parameter to `VERIFIED_SAFE`.

The designer should only set `CYCLONEII_SAFE_WRITE` parameter to entities that use the memory in the mode that is described in this section to prevent any remapping of the M4K blocks. This mode has been verified to be robust and will not exhibit write failures under any conditions.

In-System Memory Content Editor

The In-System Memory Content Editor tool will not work correctly in the affected silicon. There is no workaround for this case and the designer must use fixed silicon to use this tool.

Refer to Table 1 for a list of fixed devices.

SignalTap II Logic Analyzer

The SignalTap® II logic analyzer works correctly when compiled using the CYCLONEII_SAFE_WRITE parameter set to either PORT_SWAP or RESTRUCTURE setting. The SignalTap II logic analyzer uses simple dual-port mode and requires the port swap remapping to work correctly.

Fixed Devices Information

Fixed devices restore full functionality of the M4K blocks and do not require the Quartus II workaround. All Cyclone II designs using M4K blocks targeting fixed devices need to be recompiled in Quartus II software version 5.1 SP2 or later to function correctly and report correct timing information.

Programming File Compatibility

Beginning with version 5.1 SP2, the Quartus II software supports the logic option CYCLONEII_M4K_COMPATIBILITY. When this option is set to on, the Quartus II software will generate programming files compatible with both affected and fixed silicon. Additionally, all of the memory blocks are remapped if the Quartus II software determines the memory used in the design are in an at-risk mode. The default setting for this option is on.

To set the CYCLONEII_M4K_COMPATIBILITY variable, enter the following line in the Quartus Settings File, <*project name*>**.qsf** under the Project-Wide Assignments:

```
set_global_assignment -name
CYCLONEII_M4K_COMPATIBILITY OFF
```

When targeting fixed silicon devices, set the CYCLONEII_M4K_COMPATIBILITY variable to off and set all instances of the CYCLONEII_SAFE_WRITE parameter to NO_CHANGE to prevent the Quartus II software from remapping the M4K blocks.

When the CYCLONEII_M4K_COMPATIBILITY option is set to off, the programming files will only be compatible with revision C silicon and later for EP2C35 devices and revision B and later for EP2C5, EP2C8, EP2C20, EP2C50, and EP2C70 devices. These programming files will not configure other silicon revisions. The nSTATUS pin will drive out low and configuration will fail.

Programming file generation for fixed devices is available in Quartus II software version 6.0 or later.

Revision History

The information contained in version 1.3 of the *Cyclone II FPGA Family Errata Sheet* supersedes information published in previous versions.

Version 1.3

The following changes were made to the C*yclone II FPGA Family Errata Sheet version 1.3:*

- Updated Table 1 with an additional note.
- Added "Fixed Devices Information" section.

Version 1.2

The following changes were made to the C*yclone II FPGA Family Errata Sheet* version 1.2:

- Updated "CYCLONEII_SAFE_WRITE Parameter" on page 5.
- Updated "Special Cases" on page 8.

Version 1.1

The following changes were made to the *Cyclone II FPGA Family Errata Sheet* version 1.1:

- Updated Table 1.
- Added "M4K Memory Block Write Issue" on page 2.

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