Time Delay Digital Beamforming

**Description**

Radar systems have been using a hybrid of analog and digital beamforming (DBF). Sub-arrays of phase shifters are digitized at the sub-array output. Such systems suffer from limited bandwidth and produce only one beam at a time. DBF solves both problems. Frequency domain DBF is very efficient in resource, but inherently narrowband.

Time Delay Beamforming (TDBF), on the other hand, is natively wideband and allows a scalable number of simultaneous beams. With the advance of high density and low power FPGAs, TDBF is now possible. This reference design uses a very efficient and precise fractional delay algorithm to achieve sub-picosecond time delay. As a result, beamforming at a very fine angle can be achieved.

The design is implemented in Simulink® with Altera's DSP Builder Advanced Blockset. To test the design in hardware, other support components such as chirp generator, target range emulation, RX noise emulation, aperture tapering, and pulse compression are also implemented.

**Features**

- Highly parameterizable and efficient time delay algorithm to provide precision beam steering
- Altera’s System-in-the-Loop with MATLAB®
- Design includes chirp generator, target range emulation, rx noise emulation, and pulse compression in hardware
- Designed with Simulink/Advanced DSP Builder achieving 300MHz push button preformance
- Arbitrary fine beam angle resolution
  - 0.02 degrees implemented
  - 6-8 beams of 32 antenna in a Stratix® V

**Applications**

- Active Electronically Scanned Array (AESA)
- Radar, Sonar
- Electronic Warfare and Software Defined Radio
- Phased Array Radio Telescope


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<th>Performance Examples</th>
<th>Spec. #1</th>
<th>Spec. #2</th>
<th>Spec. #3</th>
<th>Spec. #4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample Rate (MHz)</td>
<td>300</td>
<td>300</td>
<td>267</td>
<td>250</td>
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<tr>
<td>Signal Bandwidth (MHz)</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>200</td>
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<tr>
<td>Filter Length</td>
<td>6</td>
<td>8</td>
<td>12</td>
<td>16</td>
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<td>Expected SNR (dB)</td>
<td>34</td>
<td>52</td>
<td>60</td>
<td>65</td>
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<tr>
<td>Multipliers (18x18)</td>
<td>416</td>
<td>544</td>
<td>800</td>
<td>1056</td>
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<tr>
<td>Logics (max 260k)</td>
<td>8140</td>
<td>8800</td>
<td>9300</td>
<td>10k</td>
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<td>Block RAM</td>
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<td>64</td>
<td>64</td>
<td>64</td>
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<tr>
<td>Compiled Fmax. (MHz)</td>
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<td>304</td>
<td>284</td>
<td>284</td>
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</tbody>
</table>

Performance and resource shown is for 8 simultaneous beams driving 32 antennas with varying parameters including bandwidth and SNR.

Figure 1: System-in-the-loop Digital Time Delay Beamforming Reference Design

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