



Intel Cyclone 10 GX Device Errata and Design Guidelines



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1 Intel® Cyclone® 10 GX Device Errata

This errata sheet provides information about known device issues affecting Intel® Cyclone® 10 GX devices. The table below lists specific device issues and affected Intel Cyclone 10 GX devices.

Table 1. Device Issues

Issue	Affected Devices	Planned Fix
Automatic Lane Polarity Inversion for PCIe Hard IP on page 3	All Intel Cyclone 10 GX devices	No planned fix
High VCCBAT Current when VCC is Powered Down on page 3	All Intel Cyclone 10 GX devices	No planned fix

1.1 Automatic Lane Polarity Inversion for PCIe Hard IP

For Intel Cyclone 10 GX PCIe Hard IP open systems where you do not control both ends of the PCIe link, Intel does not guarantee automatic lane polarity inversion with the Gen1x1 configuration, Configuration via Protocol (CvP), or Autonomous Hard IP mode. The link may not train successfully, or it may train to a smaller width than expected. There is no planned workaround or fix.

For all other configurations, refer to the following workaround.

Workaround

Refer to the Knowledge Database in the related links below for details to workaround this issue.

Status

Affects: All Intel Cyclone 10 GX devices.

Status: No planned silicon fix.

Related Links

[Knowledge Database](#)

1.2 High V_{CCBAT} Current when V_{CC} is Powered Down

If you power off V_{CC} when V_{CCBAT} remains powered on, V_{CCBAT} may draw higher current than expected.

If you use the battery to maintain volatile security keys when the system is not powered up, V_{CCBAT} current could be up to 120 μA, resulting in shortened battery life.



Workaround

Contact your battery provider to evaluate the impact to the retention period of the battery used on your board.

There is no impact if you connect the V_{CCBAT} to the on-board power rail.

Status

Affects: All Intel Cyclone 10 GX devices

Status: No planned silicon fix.



2 Document Revision History

Date	Version	Changes
October 2017	2017.11.06	Initial release

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